Access Transistor Underlap Optimization in 30 nm FinFET-Based 6T SRAM Using TCAD Simulation

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***Abstract*—The effect of underlap (L_{un}) on delay and leakage power in 30 nm gate length FinFET-based 6T-SRAM have been studied through extensive mixed mode-device simulations using Sentaurus TCAD. Two different cases of simulations have been carried out, namely with and without leakage current (I_{off}) constraints. The simulation results show that 'controlling L_{un}' yields more benefit when I_{off} is constrained to lower values.**

***Keywords*—FINFET, SRAM, Leakage Power, Delay, TCAD**

I. INTRODUCTION

The use of conventional planar single gate MOSFETs is becoming extremely difficult due to enhanced Short-Channel Effects (SCEs). In addition to SCEs, planar MOSFETs suffer from random dopant fluctuations in the channel area, which is believed to be the main source of threshold voltage mismatch among the devices, fabricated on the same wafer. Various structures of the Double Gate FinFETs are the most promising candidates for the replacement of conventional single gate planar MOSFETs due to their higher immunity to SCE [1]-[4]. FinFET transistor structure has been developed as an alternative to the bulk-Si MOSFET structure for improved scalability [5]. It utilizes a Si fin (rather than a planar Si surface) as the channel/body; the gate electrode straddles the fin [6]. Over the past few years, FinFETs have emerged as favorite aspirant for device scaling indicated by ITRS roadmap [7]. Static Random Access Memory(SRAM) is by far the dominant form of embedded memory found in today's Integrated Circuits (ICs) occupying as much as 60-70% of the total chip area and about 75%-85% of the transistor count in some IC products [8]. The most commonly used SRAM memory cell design uses six transistors (6-T) to store a bit which is shown in Fig. 1. Soon FinFET-based SRAMs will be seen in the market and the issues related to FinFET-based SRAM are to be explored. In this work, the underlap (L_{un}) has been taken as a parameter under our control. Among N, P and access devices the sensitive device is found out and for that device the L_{un} has been optimized. It is observed that access transistor is more sensitive when compared to other transistors. The effect of underlap on leakage power (P) and delay (D) have been studied through Technology CAD (TCAD) simulation. While doing the optimization study two different cases are considered i.e. with I_{off} and without I_{off} constraint. Next section talks about the simulator, simulation setup, simulation methodology and the parameter (delay and leakage power) extraction. Section III depicts the simulation results and their analysis. Finally section IV provides the conclusion.

II. SIMULATOR, SIMULATION METHODOOGY AND PARAMETER EXTRACTION

Sentaurus TCAD simulator from Synopsys is used for this study. This simulator has many modules and the following are used in this study.

- Sentaurus Structure Editor (SDE): To create the device structure, to define doping, to define contacts, and to generate mesh for device simulation. In Sentaurus Structure Editor, users can initialize a new model from scratch or they can load a previous model to edit, and the result can be saved for future use.
- Sentaurus Device Simulator (SDEVICE): The mixed-mode capability of Sentaurus Device allows for the simulation of a circuit that combines any number of Sentaurus Device devices. To perform mixed mode simulation of SRAM cell, shown in Fig.1 (Interconnects are assumed to have no effect on the results). Required $I_D V_G$ simulations are also done using this module [9].
- Tecplot: Tecplot SV is part of Sentaurus Workbench Visualization. It is plotting software with extensive 2D and 3D capabilities for visualizing data from simulations and experiments
- Inspect: Inspect is a plotting and analysis tool for xy data, such as doping profiles and electrical characteristics of semiconductor devices. Inspect is a tool that is used to display and analyze curves.

The physics section of SDEVICE includes the appropriate models for band to band tunneling, quantization of inversion layer charge, doping dependency of mobility, effect of high and normal electric fields on mobility, and velocity saturation.

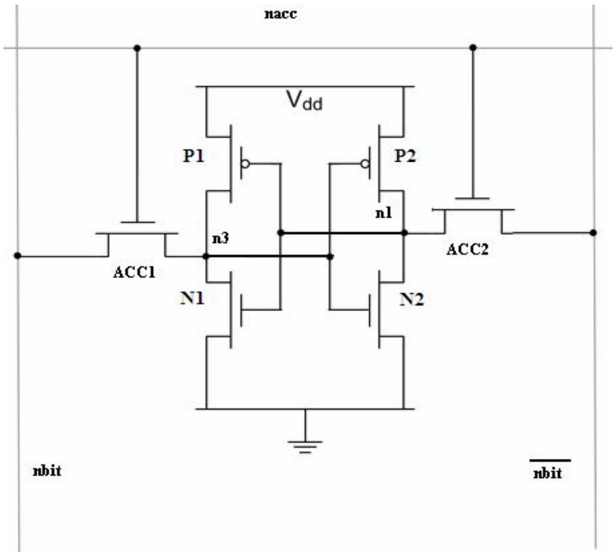

Figure 1. 6T- SRAM cell

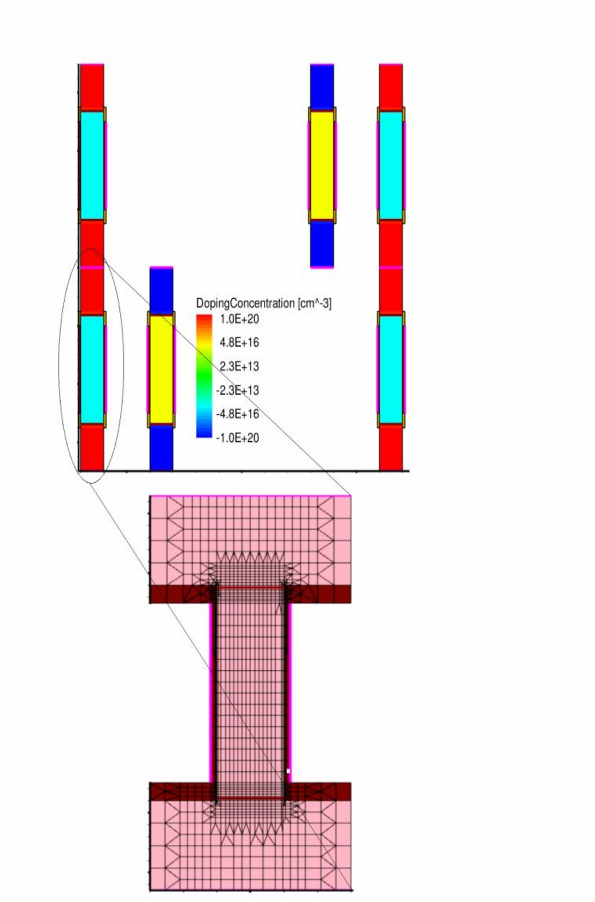

Figure 2. Structure of the Dual-Gate FinFET

SRAM structure (corresponding to Fig. 1) generated from SDE is shown in Fig. 2. Figure 2 also depicts an individual device where doping and meshing information can be noticed. Doping concentration of $1x10^{16}/cm^3$ is used for the channel, and $1x10^{20}/cm^3$ for source/drain regions. Gate electrode work functions of 4.337 eV and 4.873 eV are used for N and P type devices respectively. The various geometrical parameters in a FinFET device are shown in the schematic diagram (Fig. 3).

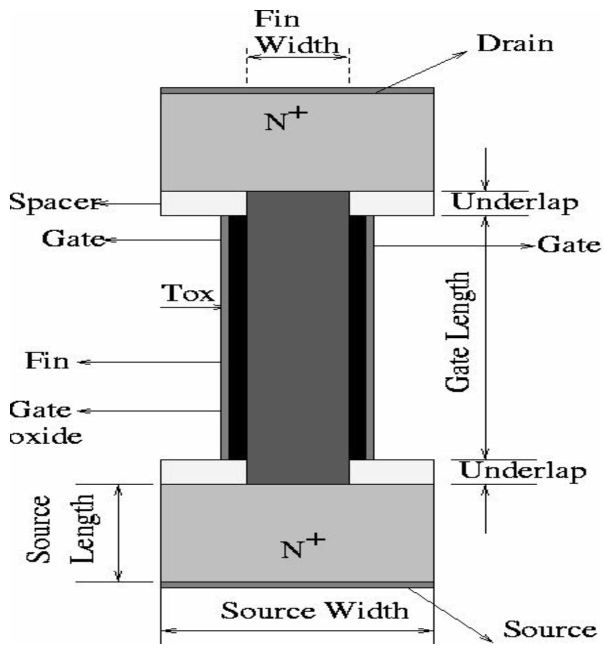

Figure 3. Schematic view of Dual-Gate FinFET

TABLE I: DEVICE DIMENSIONS

Parameter	Value
L_g	30 nm
T_{ox}	1 nm
W	10 nm
L_{un}	Varied in the range of 1 to 5 nm

TABLE II: DATA AND ACCESS PULSE TIMINGS

Pulse Name	Rise Time	Fall Time	Pulse width
nbit (data)	5ps	5ps	95ps
nacc (access)	5ps	5ps	55ps

TABLE III: VALUES OF L_{un} AND I_{off} WHEN DOPING IS KEPT CONSTANT

L_{un} (nm)	I_{off} (pA)	Doping Concentration (cm^{-3})
1	203.5	1e16
2	184.7	
3	171.9	
4	161.7	
5	154.9	

TABLE IV: VALUES OF L_{un} AND DOPING CONCENTRATIONS WHEN I_{off} CONSTRAINT IS APPLIED

L_{un} (nm)	Doping Concentration (cm^{-3})	I_{off} (pA)
1	3.15e17	150
2	6.85e16	
3	3.39e16	
4	1.78e16	
5	1e16	

Table I gives device dimension value for various geometrical parameters. Supply Voltage (V_{dd}) used in this study is 1V. Table II indicates details related to rise time, fall time, pulse width etc of access and data pulses. As already said two cases are considered in this study while dealing with the access transistors, in the first case when L_{un} changes I_{off} changes which is not constrained, and in the second case when L_{un} changes I_{off} is not allowed to change i.e. the channel doping values are modified accordingly. Table III refers to without I_{off} constraint case and gives the values of I_{off} for the various values of L_{un}. An uniform doping concentration of $1x10^{16}/cm^3$ is used for all the values of L_{un}. Table IV shows with I_{off} constraint case. In this case, as L_{un} changes the channel doping values are also altered to meet the I_{off} constraint. These are given in Table IV. I_{off} is maintained around 150 pA for all the values of L_{un}.

When access is not there during that period the current from V_{dd} is measured and multiplied by V_{dd} to extract leakage power. PMOS and NMOS gate areas are considered to be equal which means that PMOS will be the bottle neck in deciding the delay i.e. nbit/nbit going to 1 from 0. So the delay is measured when the transition is happening from 0 to 1.

III. RESULTS AND DISCUSSION

Figure 4 shows D versus L_{un} graph. When L_{un} increases, current decreases due to increase in parasitic series resistance causing D to increase, and the same can be observed in Fig. 4. It can also be observed that access transistor is more sensitive. Figure 5 and 6 show the graphs between D versus L_{un}, and P versus L_{un} respectively, without I_{off} constraint. As we can see from Fig. 5 and 6 when L_{un} increases D increases whereas P decreases. This is same as expected. Figure 7 and 8 show the graphs between D versus L_{un}, and P versus L_{un} respectively, with I_{off} constraint. As we are trying to maintain I_{off} (lower channel doping values for larger L_{un}), the mobility degradation is mitigated to some extent and it pops out as an advantage w.r.t. the delay. It can be noted from Fig. 7 that when L_{un} increases, initially we gain in terms of delay due to mobility enhancement. It should be kept in mind that we are not losing in terms of power to achieve this delay reduction (compare Fig. 6 and 8). But the further increase L_{un} causes the series resistance to go up and g_m degradation starts to dominate resulting in bad delay performance.

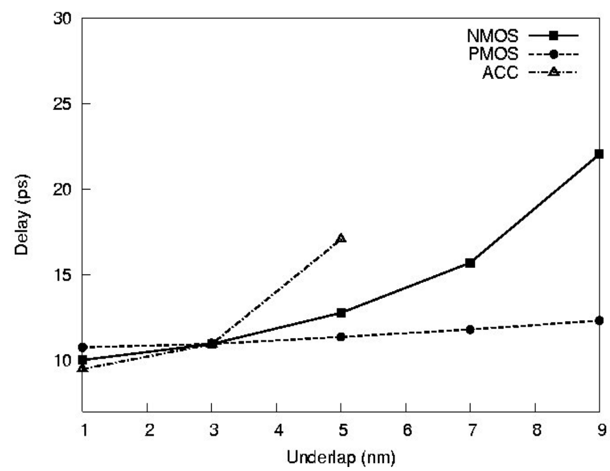

Figure 4. Delay vs L_{un}

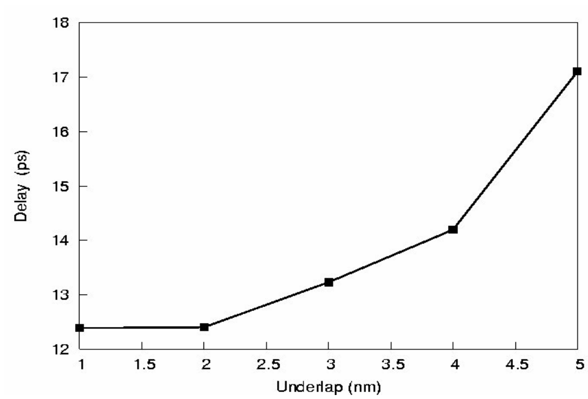

Figure 5. Delay vs L_{un} (without I_{off} constraint)

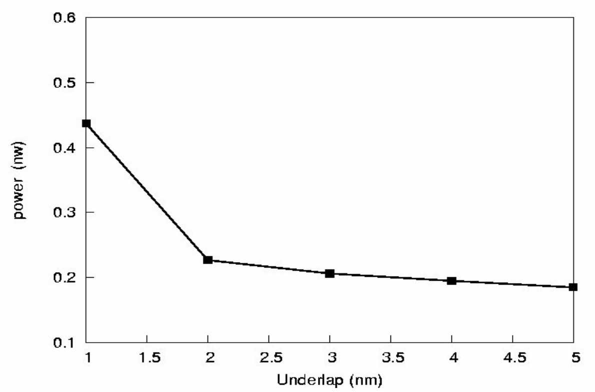

Figure 6. Leakage power vs L_{un} (without I_{off} constraint)

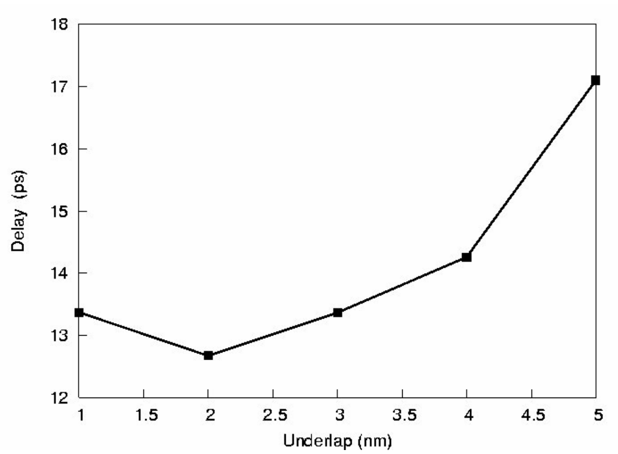

Figure 7. Delay vs L_{un} (with I_{off} constraint)

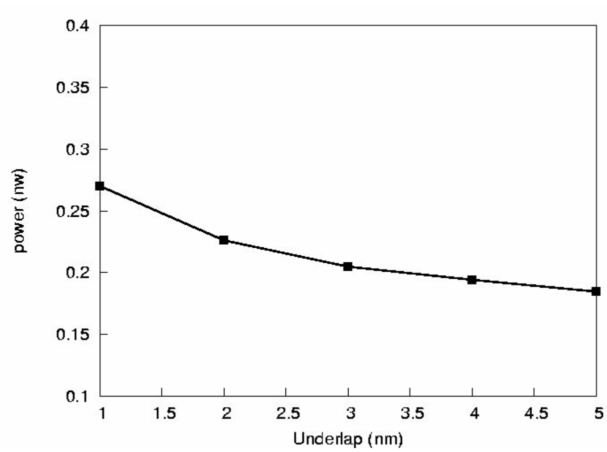

Figure 8. Variation of P vs L_{un} (with I_{off} constraint)

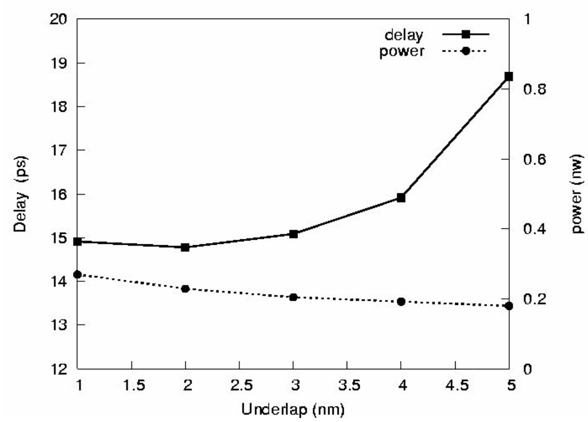

Figure 9. Leakage power and delay vs L_{un} (with I_{off} constraint-75 pA)

Figure 9 shows the variation of P and D w.r.t L_{un}, with I_{off} constraint for 75 pA. When I_{off} constraint becomes more stringent, we derive more advantage by increasing L_{un} i.e. when I_{off}=150 pA, we can decrease the leakage power by increasing L_{un} up to 2 nm, without sacrificing in delay whereas when I_{off}=75 pA, we can increase L_{un} up to 3 nm. Same can be observed from Fig. 7,8 and 9.

IV. CONCLUSION

In this work, access transistor underlap was found to be more sensitive for the SRAM cell delay and leakage power. Based on the above conclusion, underlap of the access transistor was studied with and without I_{off} constraints. We found that when I_{off} is constrained we derive advantage by increasing the underlap. Further we also found that when I_{off} is constrained to lower values more advantage can be derived by adjusting L_{un}.

V. REFERENCES

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