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An Efficient Implementation of Multiplexer Based Flip-Flop in Subthreshold Region

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***Abstract*—In this paper two different flip-flop topologies in subthreshold region of operation are examined. Designs are simulated in 90 nm process with supply voltages ranging from 200 mV to 600 mV. Ultra low power can be achieved in subthreshold region. Propagation delays and power dissipation are measured across all corners. Multiplexer based flip-flop design achieves best Power delay product 3.32 aJ and Energy delay product 0.7 yJs at supply voltage of 270 mV.**

***Index Terms*—Ultra-low Power, Subthreshold region, Propagation delay product, Energy delay product.**

I. INTRODUCTION

Digital circuits operating in sub-threshold use a supply voltage that is less than the threshold voltages of the transistors. In this region of operation, they consume less energy for active operation and they dissipate less leakage power than higher voltage alternatives, but they operate more slowly.

Subthreshold current of an MOSFET transistor occurs when the gate-to-source voltage (*VGS*) of a transistor is lower than its threshold voltage (*VTH*). When *VGS* is larger than *VTH*, majority carriers are repelled from the gate area of the transistor and a minority carrier channel is created. This is known as *strong-inversion*, as more minority carriers are present in the channel than majority carriers. When *VGS* is lower than *VTH*, there are less minority carriers in the channel, but their presence comprises a current and the state is known as *weak-inversion*. In standard CMOS design, this current is a subthreshold parasitic leakage, but if the supply voltage (*VDD*) is lowered below *VTH*, the circuit can be operated using the subthreshold current with ultra-low power consumption [1].

Operation in the subthreshold or weak-inversion region exploits the formerly parasitic subthreshold leakage current, and uses it as its primary operation current. These currents are much weaker than standard strong-inversion currents, so the time needed for charging or discharging capacitive node is longer, limiting the operation frequency of the circuit. With subthreshold region [2], [3], [4]. Subthreshold operation can substantially reduce both static and dynamic power consumption [5].

Dynamic power is greatly reduced, primarily due to the quadratic dependency on supply voltage, while static subthreshold leakage is also much lower, mainly because of the Drain-Induced Barrier Lowering (DIBL) effect. Other leakage components, such as gate tunneling, Gate-Induced Drain Leakage (GIDL) and reverse-biased diode leakage are also reduced in the subthreshold circuits.

According to the aforementioned, it could be concluded that a simple reduction of the power supply voltage of traditional circuits would achieve subthreshold operation. However, this is not the case, for power supply reduction is accompanied by a number of problems and challenges. The accompanied frequency reduction means that subthreshold operation isn't appropriate for all applications. The lower supply voltages mean lower noise margins and large vulnerability to process variations and temperature fluctuations [6], [7].The characteristics of semiconductor behavior in weak inversion are different than those in strong inversion, resulting in different sizing and ratio optimizations.

Of the various building blocks in digital designs, one of the most complex and power consuming is the Flip-Flop (FF). Several FF designs have been proposed for power reduction.

Although many of these methods have been shown to considerably reduce the power consumption, they are not necessarily suitable for operation in the subthreshold region. In addition, some of these designs require a large number of transistors for implementation, resulting in a large area, not necessarily suitable for small, low-priced systems.

This paper presents two flip-flop topologies.

A) Transmission gate based topology has been proposed and tested by Wang et al [1] modified a traditional transmission gate master-slave flip-flop by cutting off the feedback line to eliminate ratio sizing.

multiplexers, [8] the multiplexer based topology is characterized by ultra-low power dissipation and very small area at the expense of performance. Analysis of these topologies is presented across various corners for power consumption and propagation delay measurements are achieved in simulation.

Section II presents schematics of the flip-flops and circuit analysis. Simulation results of the described topologies are described in Section III with discussion on each corner i.e. Typical, SS, FF, SF, FF. Section IV concludes the paper.

II. FLIP-FLOP TOPOLOGIES AND ANALYSIS

A. Transmission gate based flip flop

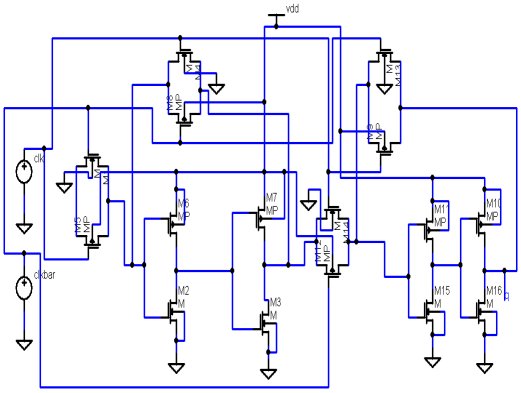


Figure1: Schematic diagram of subthreshold operated transmission gate based master slave flip–flop topology

In a normal transmission gate based flip flop operated in strong inversion region device sizing can be done with nominal size but in subthreshold region a transmission gate is inserted between the back to back connection of the inverters because the strong dependence of sub-threshold current on *VT* and temperature makes the ratio of sizing inadequate for compensating across the full process corner and temperatures ranges in sub-threshold operation. As a result, non-ratioed circuit styles provide more robust functionality in sub-threshold.

This flip-flop cut off the feedback path before writing a latch, allowing the *VGS* applied to on-transistors to increase current beyond any device off-currents even at process corners.

B. Efficient Multiplexer based flip-flop design in subthreshold region

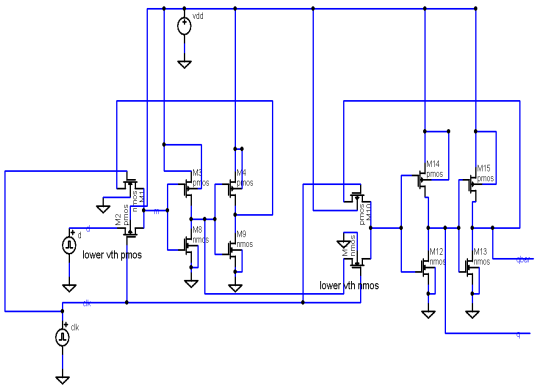


Figure 2: Multiplexer based master-slave flip-flop topology operated in subthreshold region.

Proposed flip-flop architecture proposed is a Master-Slave flip-flop based on Gate-Diffusion Input (GDI) Multiplexers [8]. GDI Multiplexers are composed of a single pair of transistors as shown in Figure 3. Thus reducing area, power consumption and clock load. This architecture isn't always suitable for strong inversion operation due to the threshold voltage drop, but this phenomenon is substantially reduced in subthreshold operation. In addition, the challenge of ratioed logic over process variations is eliminated in a multiplexer based flip-flop design.

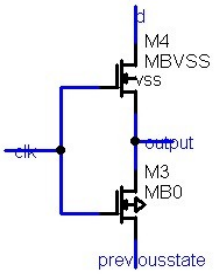


Figure 3: Gate –diffusion input based multiplexer

The design is composed of a pair of latches comprising a GDI multiplexer and a cross-coupled pair of inverters. The first multiplexer's selector is connected to the system clock and its inputs are connected to the flip-flop input (*d*) and the feedback loop. The inverted signal is the input to the second latch, with the feedback loop connected to the opposite

propagation delay due to the single inversion required before the output (*q*) is ready. In addition, cell sizing can be used to optimize the timing properties of the cell, but shouldn't affect the operation of the circuit due to incorrect ratioing or process variations. This flip-flop comprises 12 transistors, a relatively small

number, substantially reducing area and capacitance. In addition, the clock load of this design is only 4 transistor gates.

The cross-coupled inverters ensure that strong signals are assed from the multiplexers and block any reverse currents through the multiplexers.

To develop models for propagation delays, the subthreshold current of an MOS device, taking into account Drain Induced

Barrier Lowering (DIBL) is given by [2], [9]

$$I_{sub\_th} = I_0 * e^{\left(\frac{V_{GS}-V_{TH}}{nv_t}\right)} \times (1 - e^{\frac{V_{DS}}{V_T}}) \times e^{\frac{\eta V_{DS}}{nv_t}} \quad (1)$$

$$I_0 = \mu_0 C_{OX} \frac{W}{L} (n-1) v_t^2 \quad (2)$$

where *VGS* is transistor gate to source voltage, *VDS* is transistor drain to source voltage, *VTH* is threshold voltage, *Vt=kT/q* is thermal voltage, *η* is the DIBL coefficient, *n* is the subthreshold swing coefficient of the transistor, *μ0* is zero bias mobility, *Cox* is gate oxide capacitance, *W* and *L* are the width and length of the transistor.

Propagation delay for the inverters is easier to calculate and is data independent. This delay has been calculated as [10]:

$$T_{PD,INV} = \frac{KC_{load}V_{dd}}{I_0 exp\left(\frac{V_{DD}-V_{TH}}{nkT/Q}\right)} \quad (3)$$

Transistors (low threshold pmos, nmos as shown in Figure 3) were sized to minimize delay and have been implemented with a low threshold voltage, maximizing subthreshold current. Simulations show that these optimizations substantially improve performance. In addition, the VTC of the inverters following the multiplexers have been shifted to accommodate the slower output. *Inverter* after the multiplexer in master stage was shifted to speed up a '0' to '1' transition, while *Inverter* after multiplexer in slave stage was shifted to speed up a '1' to '0' transition.

III. SIMULATION RESULTS & DISCUSSION

The proposed architectures were tested and characterized in a standard 90nm Predictive technology model parameters process using the SYNOPSYS based Hspice simulator. Power supplies between 200mV and 600mV were tested. Simulations were run at the SS, SF, TT, FS and FF corners. Threshold voltage for a typical nmos transistor is 290 mVand that of a typical pmos transistor was -290 mV.

The table 1shows the flips flop characteristics at a supply voltage of 270 mV.

topology	Power [pW]	Propa-gation delay [nS]	[aJ]	[zs]
Transmission gate based flip flop	15	300	4.5	1.5
Multiplexer based flip flop topology	12	277	3.32	0.7

In Fig. 4 the delay increases as we go deeper into the subthreshold region. Delay reduces in the strong inversion region.

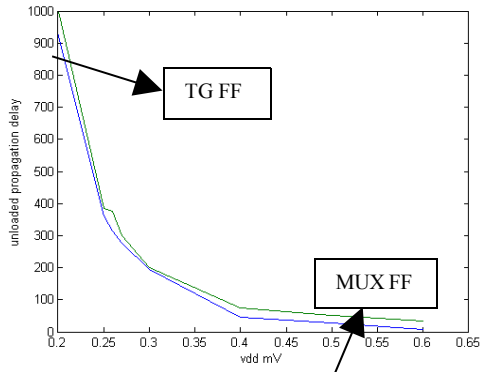


Figure 4: Typical corner t_{c-q} [nS] Vs Vdd [mV] plot

In Fig. 5 & Fig. 6 delay is more than typical corner as nmos threshold increases, pmos threshold decreases while pmos threshold increases, nmos threshold decreases respectively.

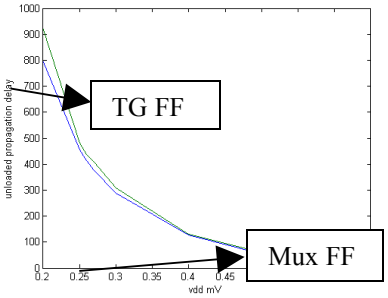


Figure 5: Slow- Fast corner t_{c-q} [nS] Vs Vdd [mV] plot

Flip-Flop	Average	Unloaded	PDP	EDP

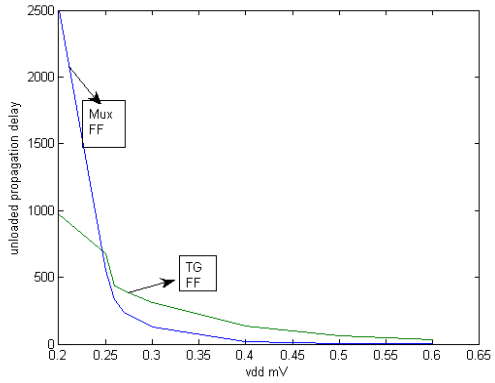


Figure 6: Fast- Slow corner t_{c-q} [nS] Vs Vdd [mV] plot

In Fig. 7 delay is maximum as nmos & pmos threshold increases.

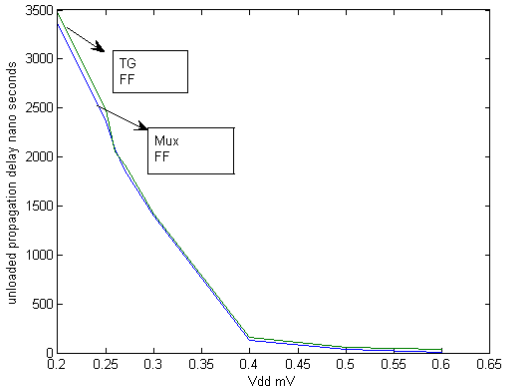


Figure 7: Slow- Slow corner t_{c-q} Vs Vdd plot

In Fig. 8 delay is minimum as nmos & pmos threshold decreases.

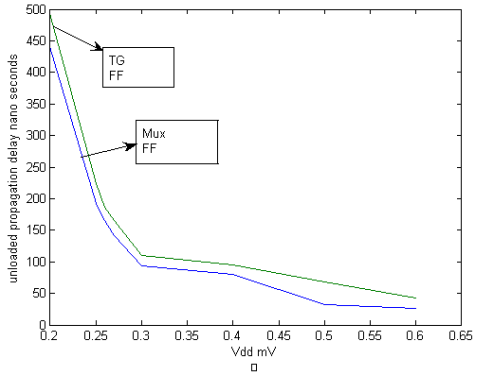


Figure 8: Fast -Fast corner t_{c-q} Vs Vdd plot

The Fig. 9 shows that the Multiplexer based flip-flop has the minimum power delay product in both regions of operation.

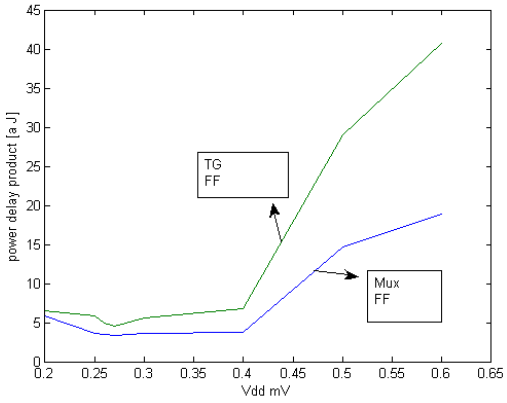
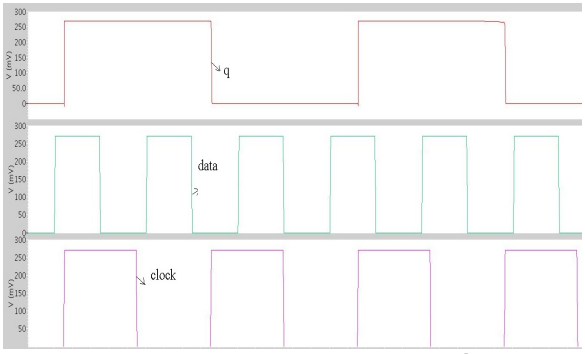
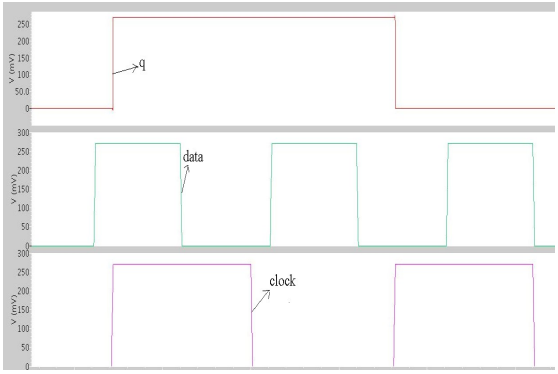


Figure 9: Power delay product Vs Vdd plot in a typical corner



Time in micro seconds→

Figure 10: Proposed Multiplexer gate based topology output



Time in micro seconds →

Figure 11: Transmission gate based flip flop topology output

For a proper comparison, all power measurements were done at the same, low frequency of 20 kHz.

IV. CONLUSION

This paper examines subthreshold operation of two different flip-flop topologies. A power dissipation as low as 6.36 Pico watts has been achieved at supply voltage of 200 mV. Low power dissipation is important in

Radio frequency identification (RFID), Low power Digital signal processor and Micro control units and lowering the supply voltage is the most effective way of decreasing the power dissipation. This comes at the cost of performance. The future research activities may include integration of the proposed Multiplexer based flip-flop design in complex digital systems, combining sequential and combinatorial logic.

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