A TRANSFORMER-LESS INVERTER WITH REDUCED COMMON MODE LEAKAGE CURRENT FOR PV APPLICATIONS

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ABSTRACT

The DC/AC inverters are used in grid-coupled Photovoltaic (PV) energy fabrication systems as the power meting out interface between the PV power source and the electric grid. Compared to the grid-coupled PV inverters that have galvanic separation (either on the DC, or on the AC side), the transformer-less PV inverters have the advantages of lower cost, higher efficiency, smaller size and lower weight. In the transformer-less topology, the common-mode (CM) ground leakage current may emerge on the parasitic capacitor between the PV panels and the ground. The transformer-less inverter is anticipated with virtual DC bus to condense the leakage current and electromagnetic losses. The PIC microcontroller generates all control signals which regulates the output voltage of DC/AC inverter. Closed loop MPPT control is also provided to achieve the desired output voltage.

Keywords—Common mode (CM) current, Transformer less Inverter, Unipolar SPWM Technique, Virtual DC Bus.

I INTRODUCTION

The distributed photovoltaic (PV) power fabrication systems have received rising attractiveness in both the commercial and housing areas. In most occasions, the inverters are used to provide for the PV power into the utility grid. It is essential for the PV inverter to be of high efficiency, due to the relatively high price of the PV panels. Small size is also firmly wanted for the low-power and single-phase systems especially when the inverters are installed indoor. In the conventional grid-connected PV inverters, either a line frequency or a high frequency transformer is utilized to provide a galvanic separation between the grid and the PV panels. Removing the isolation transformer can be a valuable way out to enhance the efficiency and condense the size and cost. If the transformer is not there, the common-mode (CM) ground leakage current may emerge on the parasitic capacitor between the PV panels and the ground. The continued existence of the Common Mode current may condense the power transfer efficiency, enhance the grid current distortion, weaken the electric magnetic compatibility, and more essentially give rise to the safety threats. The proposed scheme is to develop an improved transformer-less inverter with virtual DC bus to eliminate common mode leakage current for a PV connected power system by using unipolar sinusoidal pulse width modulation (SPWM). Other transformerless inverter topologies: (a) Karchschy inverter [8] (b) paralleled-buck inverter [9] (c) H6 inverter with capacitor voltage divider [10].

II VIRTUAL DC BUS CONCEPT

The idea of the virtual DC bus is shown in fig 2.1. By linking the grid neutral line straight to the negative pole of the PV panel, the voltage across the parasitic capacitance \( C_{PV} \) is clamped to zero. This prevents any leakage current flowing through it. With reference to the ground point N, the voltage at midpoint B is either zero or \(+V_{dc}\) according to the state of the switch bridge. The intention of introducing the virtual DC bus is to create the negative output voltage, which is essential for the function of the inverter. If an appropriate technique is used to transmit the energy between the real bus and the virtual bus, the voltage across the virtual bus can be kept identical as the real one. The positive pole of the virtual bus is linked to the ground point N, so that the voltage at the midpoint C is either zero or \(-V_{dc}\). The dotted line in the fig 2.1 indicates that this link may be realized directly by a wire or indirectly by a power switch. With points B and C coupled jointly by a smart selecting switch, the voltage at point A can be of three different voltage levels, specifically \(+V_{dc}\), zero, and \(-V_{dc}\). Since the CM current is eliminated as expected by the configuration of the circuit, there is no restriction on the modulation scheme, which means that the superior modulation technology such as the unipolar
SPWM can be used to persuade a variety of PV applications.

![Virtual DC bus concept](image1)

**Fig. 2.1 Virtual DC bus concept**

### III DERIVED TOPOLOGY AND MODULATION SCHEME

From the virtual DC bus idea, a new inverter topology is derived as a model to show the merit of the planned methodology, which is shown in Fig. 3.1. It consists of five power switches $S_1$–$S_5$ and only one single filter inductor $L_f$. The PV panels and capacitor $C_1$ form the real DC bus though the virtual DC bus is provided by $C_2$. With the switched capacitor technology, $C_2$ is charged by the real DC bus through $S_1$ and $S_3$ to maintain a constant voltage. This topology can be modulated with the unipolar SPWM. The investigation is introduced as follows.

![Proposed topology](image2)

**Fig. 3.1 Proposed topology.**

### Unipolar SPWM

The unipolar SPWM waveform of the inverter is shown in Fig. 3.2. The gate drive signals for the power MOSFET’s are generated according to the comparative value of the modulation wave $u_m$ and the carrier wave $u_c$. During the positive half grid cycle, $u_m > 0$, $S_1$ and $S_3$ are turned ON and $S_2$ is turned OFF, while $S_4$ and $S_5$ commutate complementally with the carrier frequency. The capacitors $C_1$ and $C_2$ are in parallel and the circuit rotates between the states 1 and 2 as shown in Fig. 3.1. During the negative half cycle, $u_m < 0$, $S_5$ is turned ON and $S_3$ is turned OFF. $S_1$ and $S_2$ commutate with the carrier frequency synchronously and $S_4$ commutates in balance to them. Now the circuit rotates between the states 3 and 2. At state 3, $S_1$ and $S_3$ are turned OFF while $S_5$ is turned ON. The negative voltage is generated by the virtual DC bus $C_2$ and the inverter output is at negative voltage level. At state 2, $S_1$ and $S_3$ are turned ON while $S_5$ is turned OFF. The inverter output voltage $V_{an}$ equals zero; for the moment, $C_2$ is charged by the DC bus through $S_1$ and $S_3$. 
IV OPERATION STATES OF TRANSFORMER-LESS INVERTER

The various operation states of different switches (S₁-S₅) are tabulated as below and are illustrated in figs.4.1 to 4.4.

| STATES | SWITCHES | | |
|--------|----------|---|---|---|---|
| 1      | S₁  | S₂  | S₃  | S₄  | S₅  |
|        | ON   | OFF | ON  | ON  | OFF |
| 2      | ON   | OFF | ON  | OFF | ON  |
| 3      | OFF  | ON  | OFF | OFF | ON  |
| 4      | OFF  | ON  | OFF | ON  | OFF |

**STATE I**

In the positive half grid cycle, \( u_g > 0 \), S₁ and S₃ are turned on and S₂ is turned off, while S₄ and S₅ commutate complemently with the carrier frequency. The capacitors C₁ and C₂ are in parallel and the circuit rotates between state 1 and state 2.

**STATE II**

In the negative half cycle, \( u_g < 0 \), S₅ is turned on and S₄ is turned off. S₁ and S₃ commutate with the carrier frequency synchronously and S₂ commutates in complement to them. The circuit rotates between state 3 and state 2.

**STATE III**

At state 3, S₁ and S₃ are turned off while S₂ is turned on. The voltage across capacitor C₂ generated by the virtual DC bus and the inverter output voltage are at negative level.

**STATE IV**

At state 4, S₁ and S₃ are turned off while S₂ is turned on. The inverter output voltage \( V_{an} \) equals zero, meanwhile C₂ is charged by the DC bus through S₁ and S₅.
V. CURRENT PATH DURING COMMUTATION

A derived topology main concept is to reduce the common mode current path. Here the various current paths of proposed topology during commutation is shown clearly below. It has four states of operation during the switching over of one state to other. This current path has figured out clearly.

VI. SIMULATION RESULTS

A simulink model of PIC microcontroller based transformer-less Inverter with virtual DC bus concept for a linear load- solar power system is shown in fig.6.1. Fig 6.2 and fig 6.3 shows the Input, Output voltage and current waveforms of proposed system respectively. The output of transformer-less inverter with virtual DC bus concept is fed to linear load arrangement through a well developed microcontroller based inverter drive system. The better THD range of proposed topology is shown in fig 6.4. The gating signals for MOSFET based transformerless inverter and firing pulses for the inverter are shown in fig 6.5. Fig 6.6 and 6.7 shows the reactive power generation and output voltage waveform of proposed system.

Fig 5.1 State 2

Fig 5.2 State 3

Fig 5.3 Transition state between 2 and 3

Fig 6.1 Simulink model of proposed transformer-less inverter
VII CONCLUSIONS

The idea of the virtual DC bus is proposed to resolve the Common Mode Current difficulty for the transformer-less PV-connected inverter. By linking the negative pole of the DC bus straight to the grid neutral line, the voltage on the stray PV capacitors clamped to zero. This eliminates the Common Mode current entirely. In the meantime a virtual DC bus is formed to provide the negative voltage level. The essential DC voltage is only half of the half bridge result while the presentation in eliminating the CM current is superior to the full-bridge-based inverters. Based on this design, a new inverter topology is projected with the virtual DC bus concept by adopting the switched capacitor technology. It consists of only five power switches and a single filter inductor. The proposed topology is especially fitting for the small-power single-phase applications, where the output current is comparatively small so that the extra current strain caused by the switched capacitor does not cause severe stress for the power devices and capacitors. With outstanding presentation in eliminating the Common Mode current, the virtual DC bus concept
provides an exceptional key for the transformer-less PV connected inverters. Future scope is to connect non linear load in place of resistive load with improved performances.

REFERENCES