

DESIGN OF MULTIPLYING DELAY LOCKED LOOP FOR DIFFERENT MULTIPLYING FACTORS

Aman Chaudhary, Md. Imtiyaz Chowdhary, Rajib Kar

Department of Electronics and Communication Engg.
National Institute of Technology, Durgapur-9
West Bengal, INDIA, 713209
mail.amanchoudhary@gmail.com

ABSTRACT

Clock multiplication is not possible with delay locked loops. However, ever increasing requirements for clock multiplication in analog integrated circuits has lead to the research in several avenues including ring oscillator and LC oscillator. Ring oscillators are typically used in clock multipliers of digital chips due to their smaller area, easier design, and larger frequency range compared to LC oscillators. However, ring oscillators typically exhibit much larger phase noise than their LC counterparts (for same power consumptions). This tradeoff provides an additional motivation to explore for various techniques to reduce phase noise in ring oscillators and Multiplying Delay Locked Loops (MDLL) offered an attractive alternative. In this paper, a novel method is proposed for the design of Multiplying Delay Locked Loop for different multiplying factors.

Keywords : MDLL; Phase Detector; Charge Pump; Delay Line; Select Logic; Voltage Buffer

I. INTRODUCTION

The MDLL operates by replacing every N^{th} edge of a naturally running oscillator voltage controlled oscillator (VCO) with a reference frequency edge [2], where N corresponds to the frequency multiplication factor. This allows significant suppression of jitter caused by phase noise of the VCO. Specifically, the edge multiplexing action of the MDLL rejects the VCO phase noise in a fashion similar to a type-1 order phase locked loop (PLL) with a band width of about one fourth of the reference frequency [3]. With the VCO phase noise suppressed at such a high bandwidth, the bandwidth of the tuning loop can now be lowered to better suppress the noise originating from the detector referred sources. Fig.1 shows the classical feedback approach for adjustment of V_{tune} . The key idea of this approach [4] is to use a phase detector to measure the difference in time between two appropriate edges in the system, and then use a charge pump and loop filter to integrate the resulting error signal to form V_{tune} . Ideally, V_{tune} will then be adjusted by the feedback loop until the difference in time becomes zero. proposed design. Section 4 shows the experimental results and finally section 5 concludes the paper.

II. BASIC THEORY

The MDLL consists of a three-stage differential inverter delay locked loop (DLL) whose delay is controlled by adjusting its power supply voltage using a voltage regulator [5]. The MDLL output is fed back to its input through a multiplexer [6].

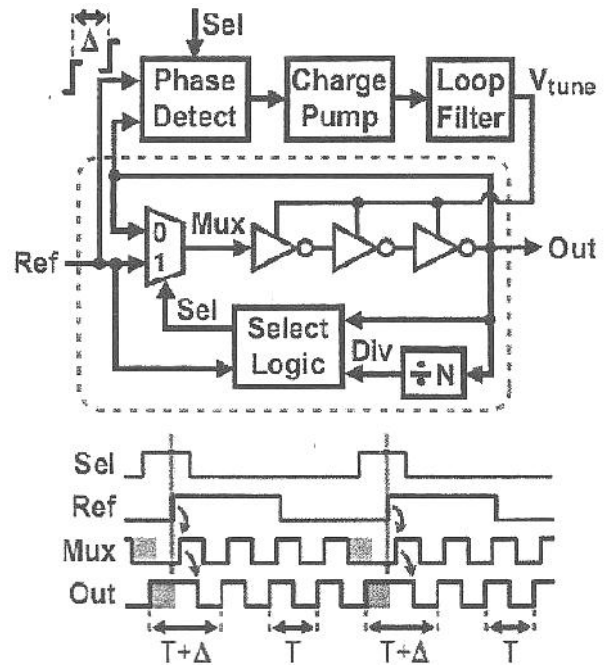


Fig. 1. MDLL Block Diagram with Output Phase Tuning

The differential 2:1 multiplexer selects between the clean reference clock r_{clk} , when the sel is asserted by select logic, and the DLL output b_{clk} , when sel signal is de-asserted. A phase detector is used to align the edge of r_{clk} to the corresponding edge of b_{clk} when multiplexing

happens. A divide by M counter provides a multiplication ratio m for the MDLL. When DLL loop is closed through the multiplexer, a ring oscillator is formed that oscillates with a period of twice to that of the delay around the DLL loop composed of the inverters and the multiplexers generating the high speed bit clock, b_{clk} . The last signal triggers the select logic that switches the multiplexer input to pass a clean reference clock edge, r_{clk} . This function resets the ring oscillator phase to phase of the clean r_{clk} edge removing any accumulated jitter over the past cycles. Therefore, the maximum number of cycles that ring oscillator accumulates jitter is limited. In contrast, a PLL typically accumulates jitter over at least 10 cycles until its loop filter can act to correct the error. Any mismatch between the swing levels, transition times, and timing alignment of the r_{clk} edge to the corresponding b_{clk} edge of the DLL stages results in final multiplied clock. Therefore, the design of the clock buffer and phase detector circuits is very critical for the MDLL performance. Fig. 2 shows the detailed timing diagram of the MDLL for two cases when the closed oscillation frequency is more than (during startup) and equal to (after settling) times that of the reference clock.

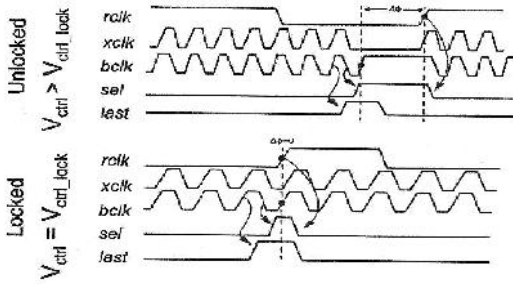


Fig. 2. Timing Diagram of the MDLL

At circuit startup, the DLL control voltage is pulled high, setting the line delay to its minimum and the ring frequency to its maximum. As a result, the b_{clk} completes its M cycles considerably before the following rising edge of r_{clk} . At the M^{th} rising transition of b_{clk} , the divide by M counter asserts the last signal at the following falling transition of b_{clk} , switching the multiplexer to its r_{clk} input. During this period the DLL stops oscillation and the multiplexer continues to select r_{clk} . The phase detector, which is also enabled by the sel pulse high, compares the corresponding rising edge of the b_{clk} with that of r_{clk} and applies a correction pulse, proportion to the phase difference between the two clock edges to a charge pump circuit that moves the loop control voltage and thus the DLL delay toward smaller phase error.

The MDLL open loop has one pole at the output of the charge pump (V_{ctrl}), and one pole at the regulated voltage node (V_{delay}) due to the large bypass capacitor

C_b . Considering that the voltage buffer is a unity gain buffer, the open loop transfer function is

$$H_o = \frac{K_p \cdot K_d \cdot M}{sC_c \cdot (sC_b \cdot R_o + 1)} \quad (1)$$

Where K_p is the charge pump gain, K_d is the DLL gain, M is the multiplication factor, and R_o is the effective ac resistance at the regulated supply node. As can be seen from the above equation (1), unlike PLL loop, the MDLL has only one pole at the origin and therefore does not require an extra zero to stabilize the feedback loop. In order to ensure that the closed loop has acceptable phase margin, the unity gain crossover frequency of the open loop transfer function $H_o(s)$ must be well below the second pole caused by the regulated supply capacitor. The worst case condition for stability arises when the loop gain is at its highest, i.e., highest multiplication factor, highest DLL and charge pump gain.

The MDLL core includes the following blocks: the multiplexed ring oscillator, divider, select logic, and reference divider apart from the feedback loop consisting the phase detector, charge pump and loop filter.

A. Delay Line

The delay elements are simple CMOS inverters whose delay is varied through supply regulation. Three delay elements connected in feedback form the ring oscillator. As control voltage approaches to the transistor threshold voltage, the gain and the supply voltage of the delay line increases significantly. To alleviate this problem, a secondary shunting inverter controlled by the programmable signal t_{rimf} is placed around the main stage inverter stage to prevent the control voltage from becoming excessively low at fast corner and low frequencies. The delay element is slower with t_{rimf} low than high. Cross coupled inverters are inserted at each delay stage to suppress skew complementary complex signals. Fig. 3 shows the schematics for the proposed delay line.

B. Select Logic

The timing of the select logic is critical at very high frequencies and can affect the MDLL jitter performance. If the select logic does not completely switch the mux input before the appropriate clock edge passes through the mux , the clock experiences a distortion that results in extra delay and therefore a phase error in that cycle. To avoid this condition, the sel signal should have fast transitions and be asserted immediately after the falling edge of the last b_{clk} and de-asserted immediately after the rising transition of r_{clk} . Therefore, the dynamic CMOS gate shown in Fig. 3 is used to increase the speed and slew rate of select logic.

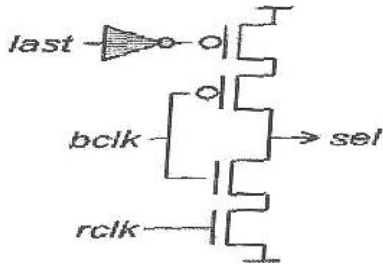


Fig. 3. Select Logic

sel is de-asserted when both r_{clk} and b_{clk} go high. This is done to guarantee a minimum *sel* pulse width and the r_{clk} rising edge advances the b_{clk} rising edge following the b_{clk} falling edge that asserted the *sel* pulse. Fig. 4 shows the acceptable and unacceptable cases of the select pulse, where the unacceptable select pulse is late with a large rising time, therefore distorting the following edge of b_{clk} .

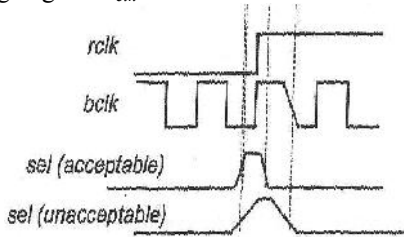


Fig. 4. Timing Diagram of the Select Logic

C. Divider

The core of the divider is formed by a D flip-flop using transmission gates and inverters in this design. The divider generates the last signal which is used by the select logic to generate the *sel* enable signal. The last signal is asserted by the divider only when the free ring oscillator finishes passing M clock pulses where M is the multiplying factor of the MDLL. In this design, factors 2 and 4 have been used. For the divide by 2 (MDLL with $M=2$), the frequency divided $clk/2$ can itself be used as the last signal as it gets asserted when two clock cycles have passed. For the divide by 4 (MDLL with $M=4$), the output is required to be NANDed with the input clock to generate the correct last signal asserting that four cycles have passed through.

III. DESIGN OF MDLL

Most of the blocks of the MDLL and DLL are common including the delay line, phase comparator, charge pump, supply voltage regulator, level buffers. The only differences are the addition of the divider, select logic, multiplexer at the beginning of the VCDL and a reduction in the number of delay cells (since it

acts like a ring oscillator, number of delay cells should be odd).

A. Delay Line

The delay elements are controlled by the control voltage generated by the charge pump block. This control voltage determines the current through the current-mirror arrangement that derives the delay-element control currents from a single control current. The output branches of the current mirrors act as the delay-element starvation devices. Device sizes are chosen to permit a small voltage drop across the starvation devices, while keeping the intermediate node capacitance reasonably small. The circuit corresponding to the current mirror arrangement and the first delay cell is shown in Fig. 5.

B. Multiplexer

It has been designed using transmission gates and inverters. The multiplexer is controlled by the *sel* asserted by the select logic. Whenever, *sel* goes high the multiplexer chooses the reference clock edge instead of the edge of the free running oscillator while when the *sel* goes low the multiplexer chooses the edge of free running oscillator. The multiplexer is used in the front of the delay line.

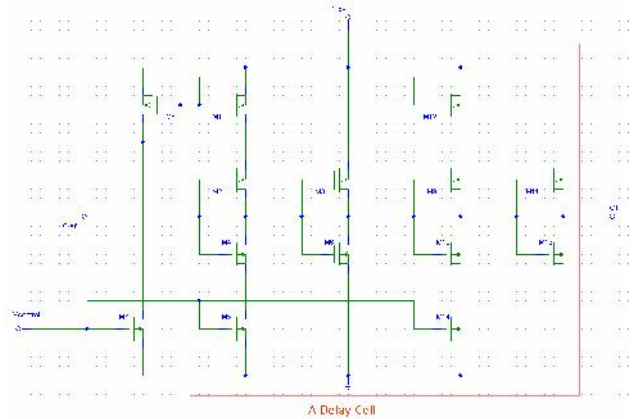


Fig. 5. A Delay Cell

C. Select Logic

Sel is asserted when the free running oscillator has finished counting M cycles and the reference clock edge has not arrived yet. After the reference edge has arrived the *sel* output is de-asserted. Here the last signal is asserted by the divider. V_{on} is the ring oscillator clock and V_m is the reference clock. Fig. 6 shows the schematic of the select logic. It is the most important part of the complete circuit and total power consumption is derived mainly by the select logic and the selectivity of various parameters is the most important factor here to decide the net performance of the circuit.

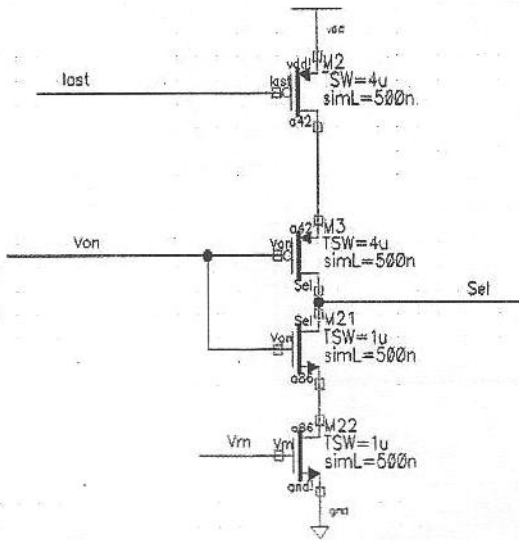


Fig. 6. Select Logic

D. Divider

Fig. 7 shows the divide by 2 circuit block. Last signal is asserted by the DFF output.

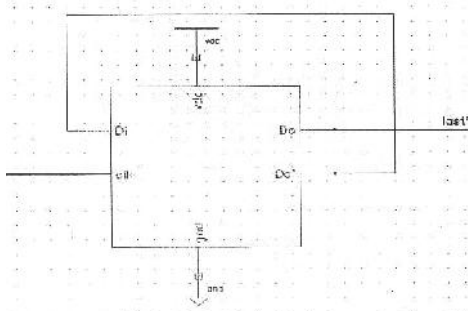


Fig. 7. Divide by 2 Circuit

Fig. 8 shows the divide by 4 schematic. To assert the last signal, the output of the two D flip-flops has counted four clock cycles (i.e., reached binary 11 states).

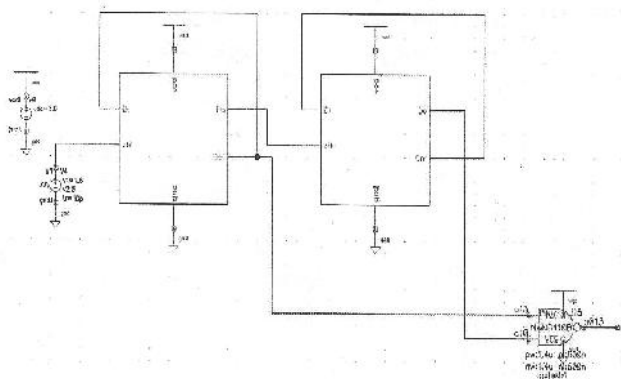


Fig. 8. Divide by 4 Circuit

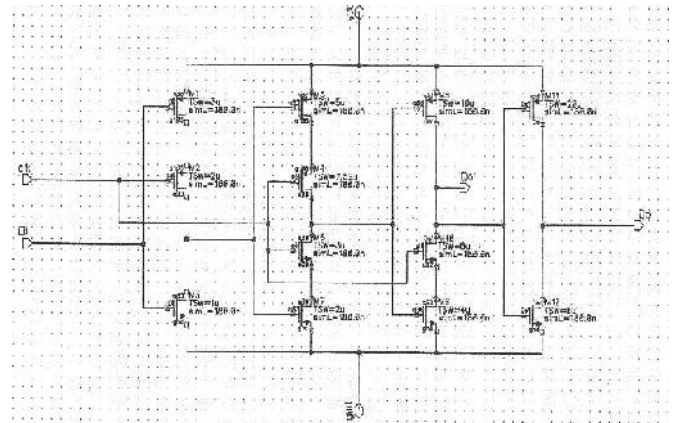


Fig. 9. D Flip-Flop Schematic

IV. LAYOUT OF MDLL

The phase comparator is the most important part of the MDLL. Fig. 10 shows the layout of the phase comparator. As the complete MDLL circuit is found to be working satisfactorily under all the process and temperature variations, we proceeded to its actual physical implementation. Fig. 11 shows the layout for the Multiple Delay Locked Loop (MDLL). After performing the Design Rule Check (DRC) and Layout Vs Schematic Check (LSC) on each of the blocks and the entire MDLL, we proceed to the RC extraction and thereby create a detailed net list for the entire circuit. Then evaluated the post-layout performance of this MDLL to verify that it satisfies the required performance criteria. The external control voltage is set at 1.2V for first 25ns and then the normal MDLL operation is enabled.

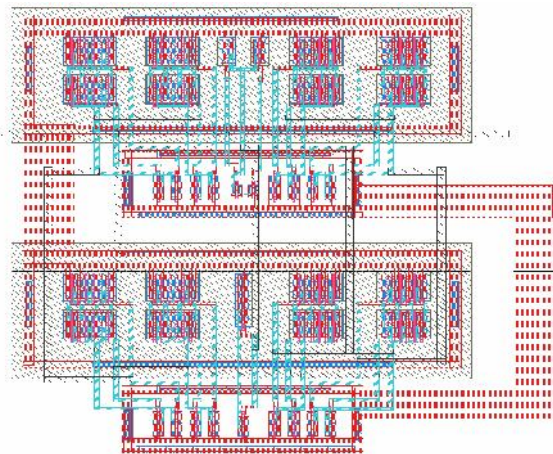


Fig. 10. Layout of the phase comparator

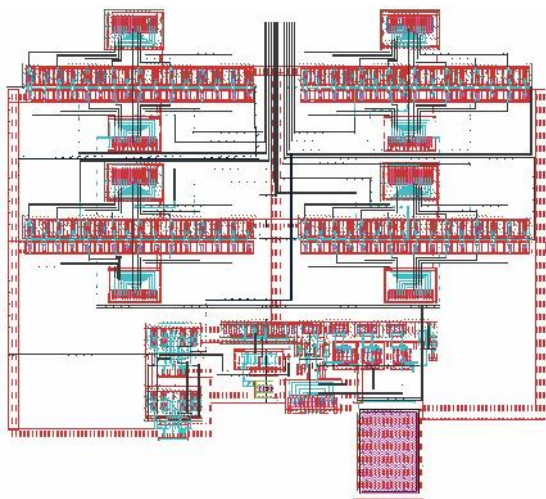
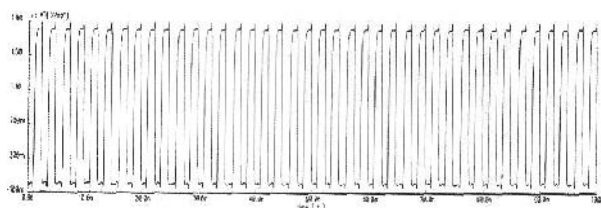


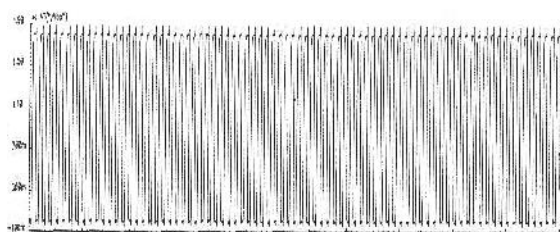
Fig. 11. Layout of Complete MDLL

V. MDLL RESULTS

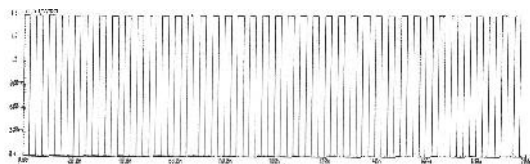
The proposed MDLL was designed for multiplication factors of 2 and 4 using the above mentioned dividers as shown below in Fig. 9. All the clock generators were tuned to give an output of 400MHz clock. However the MDLL designed could give output clocks till 700MHz. First part of the Fig. 12 represents the input, second one represents the multiplication by 4, and third one is multiplication by 2, while the last one represents the comparison with the reference input.



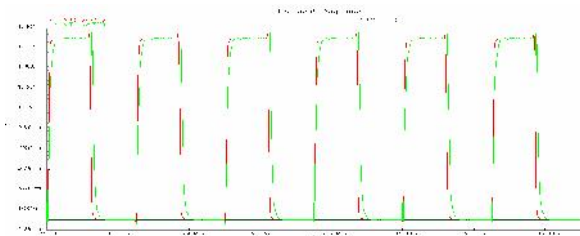
(a)



(b)



(c)



(d)

Fig. 12. (a) Input (b) Output (M=4) (c) Output (M =2) (d) Comparison with Reference Clock i.e. Responses of MDLL.

VI. CONCLUSIONS

A novel method is proposed for the design of DLL and MDLL to generate precise time intervals on chip for applications such as BIST. Since the clock generator is being used along with an ADC, it was required to make it compact and with the low power consumption. A circuit structure which performs the functionality of both the phase detector and charge pump saving area has been used. The phase comparator’s transistors were sized in such a way that locking occurs within 2-3 cycles while contemporary design takes much longer time. The sizes of the individual transistors of the delay line inverters are dependent upon the operating reference clock frequency. Since all the delay stages together need to make one clock cycle, the transistors had to be sized in such a way so that the delay stages are capable of causing the required delay. Use of a level converter and an additional buffer at the output of every delay stage ensures high output driving capability and minimum jitter.

REFERENCES

- [1] Behzad Razavi. “Design of Analog CMOS Integrated Circuits”, McGraw-Hill, 2002.
- [2] C.C. Wang, J.M. Huang, J.F. Huang, “1-Gbps LVDS Transceiver Design for LCD Panels”, IEEE Asia-Pacific Conference on Advanced System Integrated Circuits, pp. 4-5, 2004.
- [3] Daniel Eckerbert, Lars J. Svensson, and Per Larsson-Edefors, “A Mixed-Mode Delay-Locked-Loop Architecture”, Proceedings of the IEEE International Conference on Computer Design 2003 (ICCD’03), pp. 261.
- [4] Kuo-Hsing Cheng, Yu-Lung Lo, Wen-Fang Yu and Shu-Yin Hung, “A Mixed Mode Delay Locked Loop for Wide-Range Operation and Multiphase Clock Generation”, Proceedings of the 3rd IEEE International Workshop on System-on-Chip for Real-Time Applications, 2003, pp.90-93.
- [5] Ronald E. Best. “Phase-Locked Loops: Design, Simulation and Applications”, McGraw-Hill, fifth edition, 2003.
- [6] Maxim, Adrian. “Design Challenges In Multi-GHz PLL Frequency Synthesizers”, <http://www.cerc.utexas.edu/msrf>
- [7] Van Roon, Tony, “Phase Locked Loops”. 2001. <http://www.uoguelph.ca/~antoon/gadgets/pll/pll.html>.