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DESIGN OF VGA MONITOR CONTROLLER IN FPGA USING ON CHIP EMBEDDED ARRAY RAM

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ABSTRACT

VGA (Video Graphics array) as a Standard interface has already been applications widely. There are a lot of FPGA-based VGA controller designs on which, however there are still larger defects such as low-resolution display and display modules occupying large resource. In this project the design of efficient hardware architecture for VGA Monitor using VHDL as a logical means to describe the completion of high-resolution VGA control module and a resource-conserving string display module design, and provide two main modules of designing ideas and logic diagrams. It ensures a high-resolution display, the storage resources needed by the display decreased significantly. Such a design can effectively solve the problems caused by insufficient bandwidth in the displaying what More it can reduce the pressure of the CPU.

Index Term—Altera Cyclone-II -EP2C5T144C8N, block diagram, Field-programmable gate arrays (FPGAs), Very High Speed Integrated Circuit Hardware Description Language (VHDL), VGA Controller. GSM

1. INTRODUCTION

Field-Programmable Gate Arrays (FPGAs) are digital integrated circuits (ICs) that contain configurable blocks of logic along with configurable interconnects between these blocks. Specifically, an FPGA contains programmable logic components called logic elements (LEs) and a hierarchy of reconfigurable interconnects that allow the LEs to be physically connected. LEs can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

GSM/GPRS module is used to establish communication between a computer and a GSM-GPRS system. Global System for Mobile communication (GSM) is an architecture used for mobile communication in most of the countries. Global Packet Radio Service (GPRS) is an extension of GSM that enables higher data transmission rate. GSM/GPRS module consists of a GSM/GPRS modem assembled together with power supply circuit and communication interfaces (like RS-232, USB, etc) for computer. The MODEM is the soul of such modules.VGA (video graphics array) is a video display standard. It provides a simple method to connect a system with a monitor for showing information or images. As a standard display interface, VGA has been widely used. There is more and more need in displaying the result of the process in real time as the fast development of embedded system, especially the development of high speed image processing. Apart from that, display will be replacing paper for future.

2. LITERATURE SURVEY

An Efficient Architecture Design for VGA Monitor Controller. by Gudhui wang, young Guan yan Zhang. Character & Video frames are stores by external memory (u) DDRAM2 VGA control contain 2 clock frequencies for controlling pixel clock & system clock. Using VGA, the signal from the CPU is converted to VGA by the Video Adapter and sent to a monitor with VGA input. More secure signal another advantage of having VGA cable is that quality of the Video is going to be drastically improved with them

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didn't show blurry images or videos in really poor resolution.

3. ARCHITECTURE DESIGN

A. Theory of VGA Interface

There are two types VGA interface signals to display which is data signal, and the other one is control signal. Data signal have three part which is Red, Green and Blue and for control signal have two part which is Horizontal Synchronization and Vertical Synchronization. There are different frequencies of the horizontal synchronization signal and vertical synchronization signal for the changeable output resolution. Here is a table to imply the range of frequencies corresponding to these common resolutions.[1] They are just shown in Table

Table -1 List of Frequencies Corresponding to Resolutions

Resolution	Horizontal Synchronization(Hz)	Vertical Synchronization(Hz)	Pixel Clock MHz
640x480	31.496	59.940	25.175
800x600	48.077	72.188	50.000
800x600	48.875	75.000	49.500
1024x768	18.363	60.004	65.000
1024x468	56.476	70.049	75.000

In VGA control based on FPGA, we only need to consider these five signals which are horizontal synchronization signal, vertical synchronization signal, red data signal, green data signal and blue data signal. As the five signals can be sent to VGA interface from FPGA, we can make the control of VGA.[1]

B. VGA Interface Definition

VGA interface sends corresponding display signals to display through DB-15 linker which is directly connected to Monitor or LCD by monitor cable. There are 15 pinholes which are asymmetrically divided into 3 lines, and there are 5 on each line.[1] Here is Figure 2.1 showing how these pinholes are arranged.

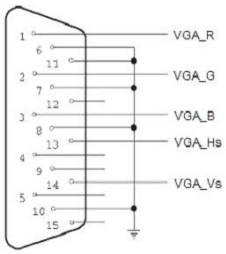

Figure- 1 VGA display port

C. VGA Color Signal

In this system, FPGA drives 5 VGA signals directly using series resistance. Every color signal is linked to a resistance serially, and a bit of color signals are made up of VGA_R, VGA_G and VGA_B. While, VGA_Hs and VGA_Vs drive level use standard LVTTL or LVCMOS3 I/O. Finally, there will be 8 kinds of color according to which level are VGA_R, VGA_GR, and VGA_BL.[1][2] They are just shown in Table-2.

Table -2 VGA Timing Control

VGA_R	VGA_G	VGA_B	Resulting Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Pink
1	1	0	Yellow
1	1	1	White

Timing of VGA signals are ruled by VESA. Here is a short introduction about how FPGA drive the VGA display with 640×480@60Hz. In the standard of VGA industry, the output frequency of pixel is 25.175MHz, and the frequencies of horizontal scan and vertical scan are 31.496 KHz and 59.940 Hz. If display receives this standard frequency, then the resolution will be 640×480, and refresh rate is 60Hz.[2] Figure and Figure 2 show us the timing of VGA's Horizontal timing and Vertical timing.

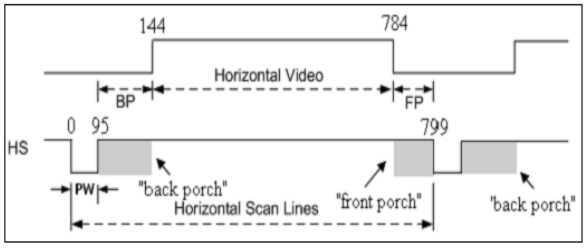

Figure:2 Horizontal Timing

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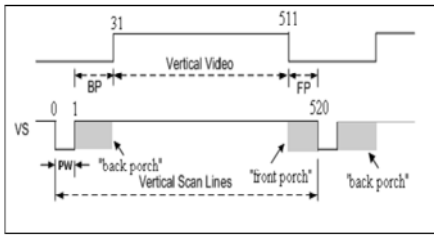

Figure- 3 Vertical Timing

D. VGA Monitor

From Figure below, it shows the VGA monitor with 640 columns by 480 rows. This VGA monitor is based on 25MHz clock. A single dot of colour on a video monitor does not impact much information. A horizontal line of pixels carries a bit more information. However, a frame composed of multiple lines can present an image on the monitor screen. A frame of VGA video typically has 480 lines and each line usually contains 640 pixels. [1]. Within the displays, current waveforms pass through the coils to produce magnetic fields, which deflect electrons beam to transverse the display in a raster pattern. The electrons move horizontally from left to the right and vertically from top to bottom across the screen as shown in Figure 2.4.[3] The scan starts from row 0, column 0 at the top left corner and moves to the right until it reaches the last column in the row. When the scan reaches the end of the row, it continues at the beginning of the next row. When the scan reaches the last pixel at the bottom right corner of the screen, it goes back to the top left corner of the screen, and repeats the scanning process again. The information only would be display when the electron is forward directions from left to the right and from top to the bottom, but when the electrons return back to the left of the top edge of the screen, the information would not be display.

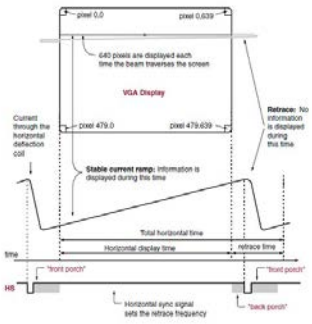

Figure: 4 VGA Monitor

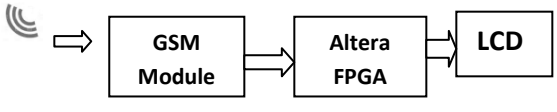

Figure:5 Proposed System Block diagram

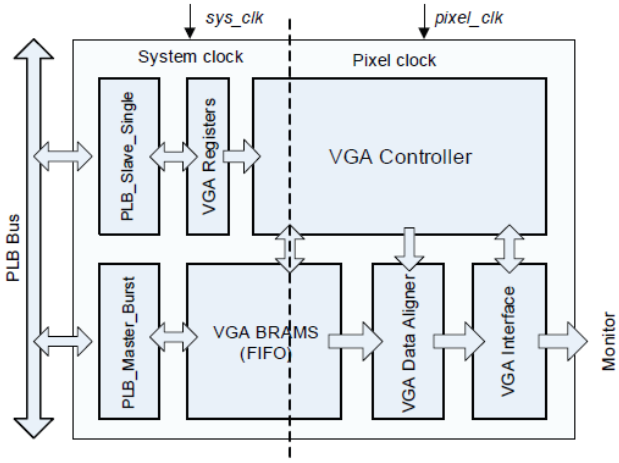

Figure:6. VGA monitor controller architecture.

There are two clock domains in this design: system clock (sys_clk) and pixel clock (pix_clk). The system clock is the source clock for the side of bus interface while the pixel clock is used for the side of VGA interface. The pixel clock frequency is required according to the display standard (as provided by [5] or [6]). It can be driven by an on-chip clock generator (using Digital Clock Manager and PLL blocks of FPGA chips) or an off-chip clock generator.

4. EXPERIMENTAL RESULTS

The function of "clock generator" block is to reduce the frequency of input clock from 50 MHz to 25 MHz meanwhile, "vga_sync" block is used to generate timing and synchronization signals. The "h_count" and "v_count" indicate the relative positions of the scans and essentially specify the location of the current pixel while the "h_sync" signal specifies the required time to scan a row, and the "v_sync" signal specifies the required time to scan the entire screen. "vga_sync" block also generates the "video_on" signal which indicates whether to enable or disable the display. Besides that, "address generator" block is used to generate address for the "img_data" block by using the "h_sync" and "v_sync" signal. "img_data" block will

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get the index data (q) from the MIF file according to the address generated. Note that the index data are connected to the "img_index" block to use as the address. The "img_index" block will get the RGB data (q) from MIF file according to the address generated (index data). The RGB data consist of 24-bits, whereas "q [23:16] ", "q [15:8]" and "q [7:0]" indicate the "R_data", "G_data" and "B_data" respectively.

A. Simulation Output

The VGA monitor controller has been implemented on different Xilinx FPGA devices with a FIFO depth of 256 bytes. To have a fair comparison of performance and resource utilization, we implemented our design and some related works (with minimized functionalities) on Xilinx Spartan3E-1600E. The result comparison is shown in Table II. Our design uses less logic and memory resources in compared with the design in (1) and (4) while it can achieve a higher performance than the others.

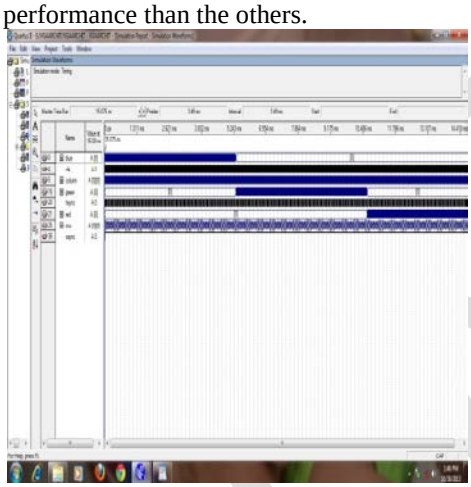

Figure.7: VGA Colour Signal

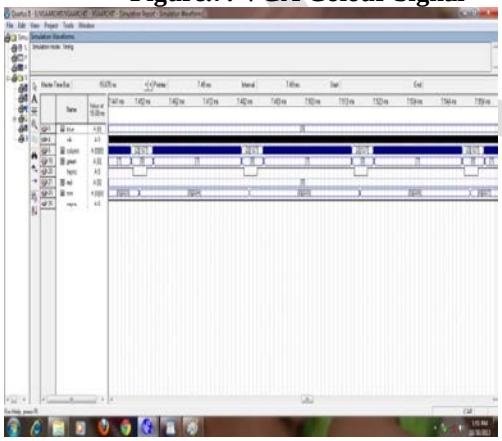

Figure.8: Timing Synchronization

5. APPLICATION OF VGA

The VGA monitor controller can be used in several systems which have video output, such as portable video systems, video games, or digital cameras with video capabilities. In this section, we provide an FPGA-based system which uses VGA monitor controller as a functional module to display visual data in both graphics mode and text mode. This system plays a role as a remote camera system.

6. CONCLUSION

We have presented efficient hardware architecture for VGA monitor controller which has a high potential to be used in Altera FPGA-based systems. The highlighted feature, make the design suitable for several FPGA devices and able to meet different requirements of targeted applications. In addition, a software library to enable text mode is also introduced. These useful features of the design have been validated through real application demonstrations.At the same time Both image and text character display simultaneously. Without using any external RAM memory. Only using On Chip embedded array memory itself displaying the features of both image and character display in the Monitor 640 x 480.

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