International Journal of Technology and Engineering System (IJTES)
Vol 8. No.1 – Jan-March 2016 Pp. 149-157
©gopalax Journals, Singapore
available at : www.ijcns.com
ISSN: 0976-1345

FPGA IMPLEMENTATION OF BIST TRANSMITTER USING ADAPTIVE SELF MIXING ENVELOPE DETECTOR

V.NIVEATHA SARO,
PG Scholar, Department of ECE,
J.J.College of Engg.&Tech,
Trichy,Tamilnadu.

V.JAYANTHI,
Assistant Professor,Department of ECE,
J.J.College of Engg. &Tech,
Trichy,Tamilnadu.

***Abstract*—While transmitting the data over communication channel, various problems such as communication error and mismatch arises. Built-in self-test (BiST) for transmitters is a desirable choice since it eliminates the reliance on expensive instrumentation to perform radio-frequency signal analysis. Existing on-chip resources, such as power or envelope detectors or small additional circuitry, can be used for BiST purposes. However, due to limited bandwidth, measurement of complex specifications, such as in-phase and quadrature (IQ) imbalance, and third-order intermodulation intercept point (IIP3) is challenging. Since IQ imbalances are most amenable for digital compensation, their characterization and monitoring are desirable. In this paper, we propose a multistep BiST technique for transmitter IQ imbalance and nonlinearity using a adaptive self mixing envelope detector. We derive analytical expressions for the output signal in linear and nonlinear modes. One of the glaring advantages of this method is that, the impairments are extracted from analyzing the response at base band frequency and thereby eliminating the need of high frequency ATE(Automated Test Equipment).**

Keywords- BIST;IQ;IIP3;ATE;
Adaptive Self Mixing Envelope Detector.

I. INTRODUCTION

With 6.2 billion mobile devices with network subscriptions today, that is expected to grow to 9 billion by 2017 [1], the market for RF devices is large and growing at a fast space. Market share in the semiconductor consumer market is highly competitive. It is primarily driven by the cost and performance of the device. Continuous CMOS scaling and including more on chip structures to form a system-on-chip (SoC) are direct affects of performance scaling. However, both SoC implementation and shrinking of devices add to stringent specification requirement. Testing these stringent specifications needs expensive test equipment which would add to the cost of the device. Test cost comprises a large share of the overall product cost for RF devices. Test cost is primarily driven by two factors, test time and test equipment cost. Efforts are consistently made to reduce test time as well as to provide test solutions on cheaper equipments. Some of the typical tests performed on RF devices are Gain, Sensitivity, Noise figure, IIP3, P1dB, I/Q imbalances. Gain and sensitivity are a measure of the strength of the signal. Noise figure is a

measure of the noise added by the device. IIP3 and P1dB are a measure of the nonlinearities introduced by the device. These parameters determine linear region of the device. I/Q imbalances determine the mismatches in I (InPhase) and Q (Quadrature) paths. These mismatches if determined can be compensated during reception. All these parameters of the device have to be determined before releasing the device to the market. All these parameters have a direct relation with respect to the proper transmission and reception of the signal. Expensive RF testers are required to perform these tests. Thus, considerable research effort needs to focus on reducing the reliance on these expensive RF testers. One of the approaches to achieve this goal is built-in-self-test (BiST). BiST circuitry can be designed using existing design components or may require additional circuitry. Additional circuitry results in increase in silicon cost. However, if simple circuits or existing resources can be used for BiST, this cost can be minimized. Generally, BiST strategies for RF devices rely on down converting the signal from RF frequency to baseband frequencies. Several techniques have been proposed to enable the RF to low frequency conversion [2]-[8]. Peak or power detectors are simple in terms of implementation [6]-[8] and introduce very little overhead. Using these kinds of detectors it is possible to measure the amplitude (or power) of the signal based on sine-wave approximation. Thus, parameters, such as 1 dB compression point, gain and third order input intercept can be measured. While the characterization of the gain, noise figure, and IIP3 has been the target of almost all prior BiST work using sensors, other important parameters of transceivers such as IQ imbalances, have not been addressed. IQ imbalances, namely IQ gain and phase mismatch, DC offsets, time skews and non linearity (IIP2 and IIP3) are detrimental to the transceiver operation and thus need to be characterized. Moreover, these parameters are amenable to digital compensation [9]-[11]. Thus, in- field measurement and monitoring of such parameters are useful in the context of circuit adaptation. A recent trend in advanced wireless transceivers is to incorporate all of the RF and mixed-signal components on a single-monolithic chip. This trend will contribute to high density system-on-chip (SoC) transceivers with higher performance and reliability. However, testing of the SoC is becoming increasingly complicated and contributes to a major bottleneck in making low-cost SoC. To solve these problems, the built-in self-test (BIST) technique in the RF and mixed-signal domain that allows SoC to evaluate its own quality without expensive external equipment is applied here as a suitable test structure on an SoC transceiver. To test a point-to-point transceiver, the loop-back technique with BIST using a spectral-signature analysis is generally used with less effort and a very small test overhead. However, this test technique has disadvantages. One is lower test coverage due to the fact that the complete transceiver is tested as a whole. Another is the need for an additional digital signal processor (DSP) due to the higher complexity of the test signature generation showed gain, noise figure, and IIP3 tests of a 900-MHz LNA using signature test with optimized test stimulus. Their technique also requires additional off-chip signature response evaluator such as fast test RF runtime system. In this project, we aim at characterizing the IQ imbalance parameters of transmitters using one self-mixing envelope detector at the end of transmitter chain. We first derive the output response of the complete model including the detector. Using this model, we devise specialized test signals so that the effect of each impairment parameter can be decoupled. The signals are applied as digital patterns at the input of the transmitters. We only use the amplitude information to determine target parameters. Amplitudes of signal components can be easily, obtained using FFT at the desired frequency locations. Using our technique, the imbalance parameters can be computed with less than 1msec test time. In order to make these

amplitude measurements, we use FFT on the low-frequency digitized signal. Digitization and signal processing can be done using already existing components in the system as most SOC's contain several house-keeping ADCs and processing units.The rest of this paper is organized as follows. The overall system model and all the impairments that have been included are presented in Section II. Section III presents the proposed method and the linear and nonlinear mode analytical equations that we use for the computations. Simulations result are presented in Section IV.

II. SYSTEM LEVEL MODEL

A.Quadrature Transmitter Architecture

In an I/Q modulation scheme, I and Q signals are modulated using sine and cosine signal that are orthogonal to each other. Thus, two uncorrelated bit streams can be modulated at the same time without increasing the bandwidth. However, orthogonal behavior of these signals is essential for the proper operation of the transmitter.A simple I/Q modulating transmitter is depicted in Fig.1. A bit stream is generally transmitted using this transmitter. The bit stream is generated by the DSP processor. The digital bit stream needs to be converted to analog signal for transmission. These signals pass through a mixer in the respective I and Q path. The mixer up converts the baseband signal to the desired RF frequency. The other signal for the mixer is generated from the Local Oscillator.

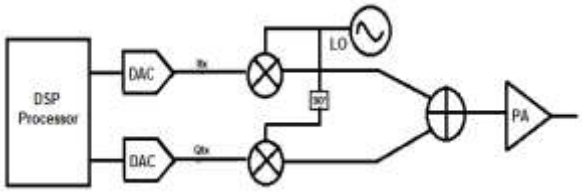

Fig.1. I/Q Modulation Transmitter

The frequency of the LO is selected based on the transmission frequency. The phase difference between the two LO signals to I and Q path should be 90 degree. This phase difference is obtained by passing the signal through a 90 degree phase shifter. The high frequency output signals from the I and Q mixers are added to form the desired RF signal. This RF signal is passed through a Power Amplifier (PA) to enable long distance transmission. This analog signal is captured using a quadrature receiver at the other end.

B. Modeling of the Transmitter

Orthogonality between I and Q channels preserves the information in limited bandwidth. Orthogonality requires that the two arms have a perfect match in gain, and exactly 90 degrees phase shift. Any deviation from this ideal point will cause leakage from I to Q and vice versa. This leakage acts as noise and degrades the transmission quality. Similarly, DC offsets generate carrier leakage and can be detrimental for the proper operation of transmission and reception. In addition to these parameters, the non-linearity of the power amplifier needs to be characterized since it both degrades modulation quality and results in spectral growth into other bands/channels.

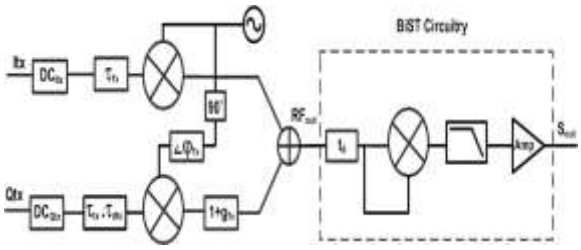

Fig. 2.Proposed transmitter model with impairments and BiST Circuitry

$$PA_{in}(t) = (I(t-\tau_{tx}) + DC_{Itx})\cos(\omega_c t) - (Q(t-\tau_{dtx}-\tau_{tx}) + DC_{Qtx})(1+g_{tx})\sin(\omega_c t + \phi_{tx}). \quad (1)$$

In this case, the PA can be modeled as

$$PA_{in}(t) = G \times PA_{in}(t) \quad (2)$$

Using the behavior of the blocks in Fig.2, the output of the detector can be expressed in terms of the transmitter inputs I(t) and Q(t) as in Eqn.(3):

$$\begin{aligned} S_{out}(t) = {} & \frac{1}{2}\left(\frac{G}{K}\right)^2 (DC_{Itx}^2 + (1+g_{tx})^2 DC_{Qtx}^2) \\ & -\left(\frac{G}{K}\right)^2 (1+g_{tx}) DC_{Itx} DC_{Qtx} \sin(\phi_{tx}) \\ & +\left(\frac{G}{K}\right)^2 (DC_{Itx} - (1+g_{tx}) \sin(\phi_{tx}) DC_{Qtx}) \\ & \times I(t - \tau_{tx} - t_d) \\ & +\left(\frac{G}{K}\right)^2 (1+g_{tx})((1+g_{tx}) DC_{Qtx} - DC_{Itx} \sin(\phi_{tx})) \\ & \times Q(t - \tau_{tx} - \tau_{dtx} - t_d) \\ & +\left(\frac{1}{2}\right)\left(\frac{G}{K}\right)^2 I^2(t - \tau_{tx} - t_d) + \frac{1}{2}\left(\frac{G}{K}\right)^2 (1+g_{tx})^2 \\ & \times Q^2(t - \tau_{tx} - \tau_{dtx} - t_d) \\ & -\left(\frac{G}{K}\right)^2 (1+g_{tx}) \sin(\phi_{tx}) I(t - \tau_{tx} - t_d) \\ & \times Q(t - \tau_{tx} - \tau_{dtx} - t_d). \end{aligned} \quad (3)$$

TABLE I. Parameter definition

Parameter	**Symbol Representation**
Gain Mismatch	g_{tx}
Phase mismatch	φ_{tx}
TX DC Offsets	$DC_{Itx,}$ DC_{Qtx}
Baseband Time Skew	□ dtx
Baseband Delay	□tx
Self Mixing Delay	*t* d
Path Gain	G,G2,G3
Self Mixing Attenuation	K

C. BIST Architecture Envelope Detector

Generally in RF BiST techniques, the high frequency circuit response is converted into a low frequency form which is easier to analyze on chip. The conversion needs to carry all the information pertaining to the desired parameters. For this purpose, a self-mixing envelope detector is used as shown in Fig. 3. This detector basically multiplies the transmitter output with itself, generating a low-frequency component, and a high frequency component. The high frequency component is filtered by the Low Pass Filter. Thus, such existing detectors can be used for BiST purposes. The output signal from the detector is digitized and analyzed. A generic on-chip ADC and processor can be used for this purpose.

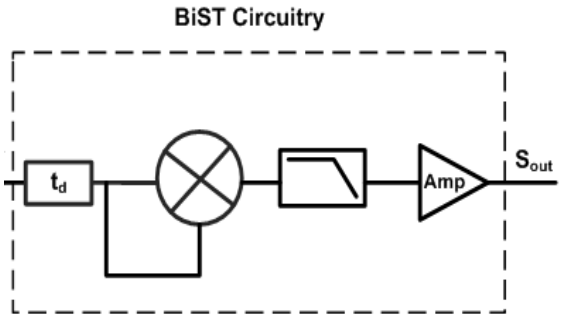

Fig. 3. BiST circuitry

III. EXTRACTION OF IMPAIRMENTS

Due to the separation of the effect of different non-idealties on different frequency locations, we can use the amplitude of the frequency terms to compute these impairments and solve for them mathematically. Equation (4) shows the amplitude expression for each of the frequency locations, while A is the amplitude of the input signal on both arms.

$$
\begin{aligned}
A_{DC} &= \frac{1}{2}\left(\frac{G}{K}\right)^2 \\
&\quad \times\left[\frac{A^2}{2}+\frac{A^2}{2}(1+g_{tx})^2+DC_{Itx}^2+(1+g_{tx})^2DC_{Qtx}^2\right] \\
&\quad -\left(\frac{G}{K}\right)^2(1+g_{tx})DC_{Itx}DC_{Qtx}\sin(\phi_{tx}) \\
A_{\omega_1} &= A\left(\frac{G}{K}\right)^2\left[DC_{Itx}-(1+g_{tx})DC_{Qtx}\sin(\phi_{tx})\right] \\
A_{\omega_2} &= A\left(\frac{G}{K}\right)^2(1+g_{tx})\left[(1+g_{tx})DC_{Qtx}-DC_{Itx}\sin(\phi_{tx})\right] \\
A_{2\omega_1} &= \frac{A^2}{4}\left(\frac{G}{K}\right)^2 \\
A_{2\omega_2} &= \frac{A^2}{4}\left(\frac{G}{K}\right)^2(1+g_{tx})^2 \\
A_{\omega_1+\omega_2} &= \frac{A^2}{2}\left(\frac{G}{K}\right)^2(1+g_{tx})\sin(\phi_{tx}) \\
A_{\omega_1-\omega_2} &= \frac{A^2}{2}\left(\frac{G}{K}\right)^2(1+g_{tx})\sin(\phi_{tx}). \qquad (4)
\end{aligned}
$$

A. Linear Parameter Extraction

With the above input signal, in the linear mode, we have seven frequency locations to analyze, as shown in (4). We also have five unknowns (G/K, g_{tx}, φ_{tx}, DC_{Itx}, and DC_{Qtx}). However, as (4) shows, expressions for the two frequencies ($\omega_1-\omega_2$) and ($\omega_1+\omega_2$) have the same amplitude, so they provide only one linearly independent equation. The dc term is unreliable even though it provides more equations. The DUT local oscillator leakage can be mixed with itself and produces an undesired dc component that can alter the accuracy of the computation. In addition, dc term may be corrupted by any dc offset that is generated by the detector, which is not included in the model. Thus, (4) yields five usable linearly independent equations with five unknowns. We also observe that by taking a step-by-step approach, the unknowns can be analytically solved for the following.

a) Computation of Gain, Phase mismatch and DC offsets:

Step 1: The path gain is extracted using the amplitude of the ($2\omega_1$)term as in Eqn. (6):

$$\frac{G}{K}=2\sqrt{\frac{A_{2W1}}{A^2}} \qquad (5)$$

Step 2: The amplitude at the 2 ω_2 frequency along with the already computed path gain are used to compute the gain mismatch as shown in Eqn. (6).

$$g_{tx}=2\sqrt{\frac{A_{2W_2}}{A^2\left(\frac{G}{K}\right)^2}}-1. \qquad (6)$$

Step 3: Eqn. (3) shows that the remaining unknown in the amplitude of the terms at ($\omega_1+\omega_2$) or ($\omega_1-\omega_2$) frequencies is the phase mismatch.It can be computed using Eqn. (7).

$$\varphi_{tx}=\sin^{-1}\left(\frac{2A_{w1-w2}}{A^2\ (\frac{G}{K})^2(1+g_{tx})}\right) \qquad (7)$$

Step 4: In order to solve for the DC offsets, we make use of information at the frequency locations ω_1 and ω_2. Eqn. (8) shows the mathematical expression for I and Q DC offset computation.

$$DC_{Itx}=\frac{A_{W1}(1+g_{tx})+A_{w2}\sin(\varphi_{tx})}{A(\frac{G}{K})^2\ (1+g_{tx})\cos^2(\varphi_{tx})}$$

$$DC_{Qtx} = \frac{A_{W2+}A_{W1}(1+g_{tx})\sin(\varphi_{tx})}{A(\frac{G}{K})^{2}(1+g_{tx})^{2}\cos^{2}(\varphi_{tx})} \quad (8)$$

B. Computation of Time Skews

If we measure these delays, the time skews can be calculated simply as the difference between the phases of the signal components at $2\omega_1$ and $2\omega_2$ frequencies as Eqn. (9):

$$\tau_{dtx} = \frac{\arg(2_{w1})}{2_{w1}} - \frac{\arg(2_{w2})}{2_{w2}} \quad (9)$$

C. De-embedding Gain Fluctuations

In some cases, the amplifiers used in the path either as a part of the CUT or as a part of the BiST circuit may exhibit fluctuations in the gain. This is more of a problem for baseband operation where the test signals are spread through a large portion of pass band as opposed to RF operation where several megahertz separations are not significant. To prevent the gain fluctuations from corrupting the computation of the parameters of interest, it may be necessary to parameterize gain at multiple frequency locations. Note that in our technique, we have five frequency locations in linear mode and one in nonlinear range to characterize. A carefully crafted test signal is used to characterize the parameter G/K at the desired frequency locations before moving into the other steps of computation. Thus, step 1 is repeated five times to obtain the G/K variable to be used in steps 2–4. In characterizing process, we have to make sure to excite the amplifier in its linear range.Otherwise, gain compression effect causes wrong measurement for G/K.

D. Nonlinear Parameter Extraction

Increasing input power, the PA operates in its nonlinear region. It is important to measure the third-order intercept point (IP3) of the PA to make sure that in the normal mode of operation, the device is not affected with gain compression or undesired frequency components of the signal. The amplitude of the IP3 at the input (IIP3) is defined as

$$A_{IIP3} = \sqrt{\frac{4}{3}\frac{|G|}{|G3|}} = \sqrt{\frac{4}{3}\frac{\left|\frac{G}{K}\right|}{\left|\frac{G3}{K}\right|}} \quad (10)$$

Where G refers to the first-order gain and G3 is the third order gain coefficient. Here, we take both coefficients in the scalar mode. The AM/AM and AM/PM distortion caused by the complex coefficients of the PA will not affect the remaining models if we ensure that we:

*C*1) do not use G/K measurement in the nonlinear mode subject to AM/AM distortion;
C2) do not use any information of the phase subject to AM/PM distortion.

In the nonlinear region, the PA is modeled as a third-order polynomial as

$$PA_{out}(t) = G\,X\,PA_{in}(t) + G_3\,X\,PA_{in}^{3}(t) \quad (11)$$

Equation (12) shows the PA output response in closed form. I(t) and Q(t)are to be substituted with the test signal and the response has to be expanded to determine the frequency-domain representation of the signal.

$$\begin{aligned}&\mathrm{PA}_{\mathrm{out}}(t)\\&= G \times [(I(t-\tau_{\mathrm{tx}}) + \mathrm{DC}_{\mathrm{Itx}})\cos(\omega_c t)\\&\quad -(Q(t-\tau_{\mathrm{dtx}}-\tau_{\mathrm{tx}}) + \mathrm{DC}_{\mathrm{Qtx}})(1+g_{\mathrm{tx}})\sin(\omega_c t+\phi_{\mathrm{tx}})]\\&\quad + G_3 \times [(I(t-\tau_{\mathrm{tx}}) + \mathrm{DC}_{\mathrm{Itx}})\cos(\omega_c t)\\&\quad -(Q(t-\tau_{\mathrm{dtx}}-\tau_{\mathrm{tx}}) + \mathrm{DC}_{\mathrm{Qtx}})(1+g_{\mathrm{tx}})\sin(\omega_c t+\phi_{\mathrm{tx}})]^3.\end{aligned} \quad (12)$$

Equation (13) shows the amplitude of 4 ω_1

$$\begin{aligned}A_{4\omega_1} = \frac{1}{k^2}\Bigg[&\frac{3}{32}A^4\Bigg(G_1G_3 + \frac{5}{8}A^2G_3^2 + \frac{25}{4}\mathrm{DC}_I^2G_3^2\\&+\frac{15}{8}A^2G_3^2(1+g_{\mathrm{tx}})^2\\&+\frac{15}{4}\mathrm{DC}_q^2G_3^2(1+g_{\mathrm{tx}})^2\Bigg)\\&-\frac{30}{128}A^4G_3^2(1+g_{\mathrm{tx}})^2\cos(2\phi_{\mathrm{tx}})\left(\frac{A^2}{2}+\mathrm{DC}_q^2\right)\\&-\frac{75}{64}A^4\mathrm{DC}_I\mathrm{DC}_qG_3^2(1+g_{\mathrm{tx}})\sin(\phi_{\mathrm{tx}})\Bigg].\end{aligned} \quad (13)$$

1)Computation of IIP3

The amplitude of the signal in each frequency location is analyzed to find a simple useful equation to compute G_3/K, which satisfies the two constraints C1) and C2). By going through each frequency component of the entire composite signal, we observe that the amplitude at A_{6w1} is only a function of input amplitude (A) and G_3/K as

$$\mathrm{A_{6w1}} = \frac{5}{512}\left(\frac{\mathrm{G3}}{\mathrm{K}}\right)^2 \mathrm{A^6} \quad (11)$$

Thus, the third-order coefficient can be computed as follows:

$$\mathrm{f}\left(\frac{\mathrm{G3}}{\mathrm{K}}\right) = \sqrt{\frac{512}{5}\frac{\mathrm{A_{6w1}}}{\mathrm{A^6}}} \quad (15)$$

Thus, IIP3 computation precision is not affected by linear impairments of the path.

IV. RESULTS AND DISCUSSIONS

This chapter describes the design and implementation of BIST transmitter on FPGA. It describes, in brief, about simulation had been done in XILINX Software using VHDL Language and implementation done using ALTERA FPGA BOARD. System development is done in incremental steps. At each successive step, test cases are developed and simulation is done to verify the correct behavior. At any step, if any violation from the expected behavior is found, the design entry is modified to rectify the violation and the process is repeated until all design expectations are met. Initially, after completing the design entry, simulation is done using several test benches.

4.1 Output of BIST transmitter

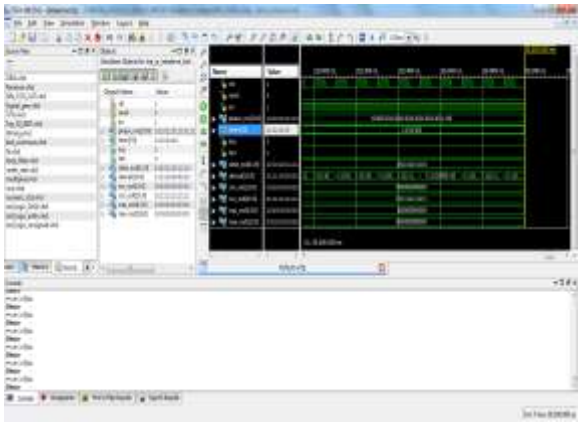

Figure 4.1:Simulation Result of BIST transmitter.

V . CONCLUSION

A BiST solution for transmitter IQ imbalances and nonlinearities measurement was proposed. Testing high frequency devices requires using expensive RF measurement equipment. We design a BiST circuitry to convert this signal to a simpler form. For low-frequency conversion, we use

a adaptive self mixing envelope detector. The proposed BiST circuitry along with designed test signal enables us to derive the transmitter impairment measurement with low computational complexity. The frequency domain information of the envelope signal is used to mathematically solve for the I/Q imbalances and nonlinearities. Simulations confirm the accuracy of the technique.

ACKNOWLEDGMENT

Our thanks to the experts who have contributed towards development of the paper.

REFERENCES

[1] M. Windisch and G. Fettweis, "Adaptive I/Q imbalance compensation in low-IF transmitter architectures," in Proc. IEEE Veh. Technol. Conf.(VTC-2004), Los Angeles, CA, Sep. 2004, pp. 2096–2100.

[2] S. Bhattacharya, A. Chatterjee, "Use of Embedded Sensors for Built-in-Test RF Circuits" in International Test Conference 2004.

[3] S. Bhattacharya, A. Chatterjee, "A Built-in Loopback Test Methodology for RF Transceiver Circuits using Embedded Sensor Circuits" in 13th Asian Test Symposium, November 2004, pp. 68–73.

[4] H. Hsieh, L. Lu, "Integrated CMOS Power Sensors for RF BIST Applications" in 24th IEEE VLSI Test Symposium, May 2006.

[5] Y. Huang, H. Hsieh, L. Lu, "A Low-Noise Amplifier with Integrated Current and Power Sensors for RF BIST Applications," VLSI Test Symposium, IEEE, 2007.

[6] M.J. Barragan, R Firoelli, D Vazquez, A Rueda, J.L. Huertas, "Low- Cost Signature Test of RF Blocks Based on Envelope Response Analysis" in IEEE European Test Symposium, (ETS), May 2010, pp.55–60.

[7] K. Yanagisawa, N. Matsuno, T. Maeda, S. Tanaka, "A New DC Offset and I/Q-Mismatch Compensation Technique for a CMOS Direct- Conversion WLAN Transmitter" in IEEE Microwave Symposium, June 2007.

[8] D. Han, A. Chatterjee, "Robust Built-in Test of RF ICs Using Envelope Detectors" in 4th Asian Test Symposium, December 2005.

[9] M. Valkama, M. Renfors, and V. Koivunen, "Advanced methods for I/Q imbalance compensation in communication receivers," IEEE Transactions on Signal Processing, pp. 2335–2344, Oct 2001.

[10] E. Erdogan and S. Ozev, "Detailed characterization of transceiver parameters through loop-back-based BIST," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, pp. 901–911, 2010.

[11] A. Banerjee, V. Natarajan, S. Sen, A. Chatterjee, G. Srinivasan, and S. Bhattacharya, "Optimized Multitone Test Stimulus Driven Diagnosis of RF Transceivers Using Model Parameter Estimation," in International Conference on VLSI Design, January 2011, pp. 274 – 279.45

[12] F. Poehl, F. Demmerle, J. Alt, H. Obermeir, "Production Test Challenges for Highly Integrated Mobile Phone SOCs- A Case Study" in 15th IEEE European Test Symposium, May 2010.

[13] L. Dermentzoglou, A. Arapoyanni, and Y. Tsiatouhas, "A Built-In-Test Circuit for RF Differential Low Noise Amplifiers," IEEE Transactions on Circuits and Systems I: Regular Papers, pp. 1549–1558, July 2010.

[14] A. Gopalan, T. Das, C. Washburn, and P. R. Mukund, "An Ultra- Fast, On-Chip BiST for RF Low Noise Amplifiers." in VLSI Design, 2005, pp. 485–490.

[15] S. Sermet Akbay and A. Chatterjee, "Built-in test of RF components using

mapped feature extraction sensors," in 23rd IEEE VLSI Test Symposium, May 2005, pp. 243–248.
[16] A. Valdes-Garcia, W. Khalil, B. Bakkaloglu, J. Silva-Martinez, and E. Sanchez-Sinencio, "Built-in Self Test of RF Transceiver SoCs: from Signal Chain to RF Synthesizers," in IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, June 2007, pp. 335–338.
[17] D. Lupea, U. Pursche, and H.-J. Jentschel, "RF-BIST: loopback spectral signature analysis," in Design, Automation and Test inEurope Conference and Exhibition, 2003, pp. 478–483.
[18] J.-Y. Ryu, B. Kim, and I. Sylla, "A new low-cost RF built-in self test measurement for system-on-chip transceivers," IEEE Transactions on Instrumentation and Measurement, pp. 381–388, April 2006.
[19] M. Barragan, R. Fiorelli, D. Vazquez, A. Rueda, and J. Huertas, "On-chip characterization of RF systems based on envelope response analysis," Electronics Letters, pp. 36–38, July 2010.
[20] D. Han, S. Bhattacharya, and A. Chatterjee, "Low-cost parametric test and diagnosis of RF systems using multi-tone response envelope detection," Computers Digital Techniques, pp. 170–179, May 2007.
[21] J. de Witt and G.-J. van Rooyen, "A blind I=Q imbalance compensation technique for direct-conversion digital radio transceivers," IEEE Transactions on Vehicular Technology, pp. 2077–2082, May 2009.
[22] A. Tarighat, R. Bagheri, and A. Sayed, "Compensation schemes and performance analysis of IQ imbalances in OFDM receivers," IEEE Transactions on Signal Processing, pp. 3257–3268, Aug. 2005.
[23] E. S. Erdogan, Sule Ozev, "Single-Measurement Diagnostic Test Method for Parametric Faults of I/Q Modulating RF Transceivers," in Proc. 26th VLSI Test Symp., May 2008.
[24] B. Razavi, "RF Microelectronics," Prentice Hall, NJ 1998.
[25] Thomas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits," Cambridge University Press, second edition.
[26] G. Roberts, F. Taenzler, M. Burns, "An introduction Mixed-signal IC Test and Measurement", Oxford University press, second edition.